



SPECIFICATION FOR TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HG MODEL : HG050HD030T01

Preliminary Specification

Final Specification

Customer Confirmation column:

Approved by : _____ Dept. : _____ Data : _____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by



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1. GENERAL INFORMATION

1.1 features

- 1) Structure: AMOLED oncell+IC+FPC+LENS
- 2) IPS Type LCD 720 dot-segment and 1280 dot-common outputs
- 3) 16.7M Color can be selected by software
- 4) White LED back light
- 5) MIPI-4 interface
- 6) Operation Temperature : -40~65°C
- 7) Storage Temperature : -55~70°C
- 8) CTP cover lens : Corning
- 9) CTP structure : oncell
- 10) LED life time: -/

1.2 General specification

Item of	Contents	Unit
Panel Size	5.0	inch
LCD Type	a-si/TRANSMISSIVE	/
Display mode	Normally Black	/
Pixel arrangement	720*3 (RGB)*1280	Dots
Pixel pitch (W*H)	28.65 (H)*85.95 (V)	um
Active Area	61.884 (H)*110.016 (V)	Mm
Module area (W*H*T)	74.8 (H)*128.5 (V)*2.09 (T)	Mm
Recommended Viewing Direction	ALL	0' clock
LCM IC	RM67295	/
TP IC	TBD	
Interface	MIPI-4	/
Luminance for LCM+TP	320	cd/m2
NTSC	110	%
Weight	TBD	g



3. I/O CONNECTION & BLOCK DIAGRAM

3.1 I/O connection

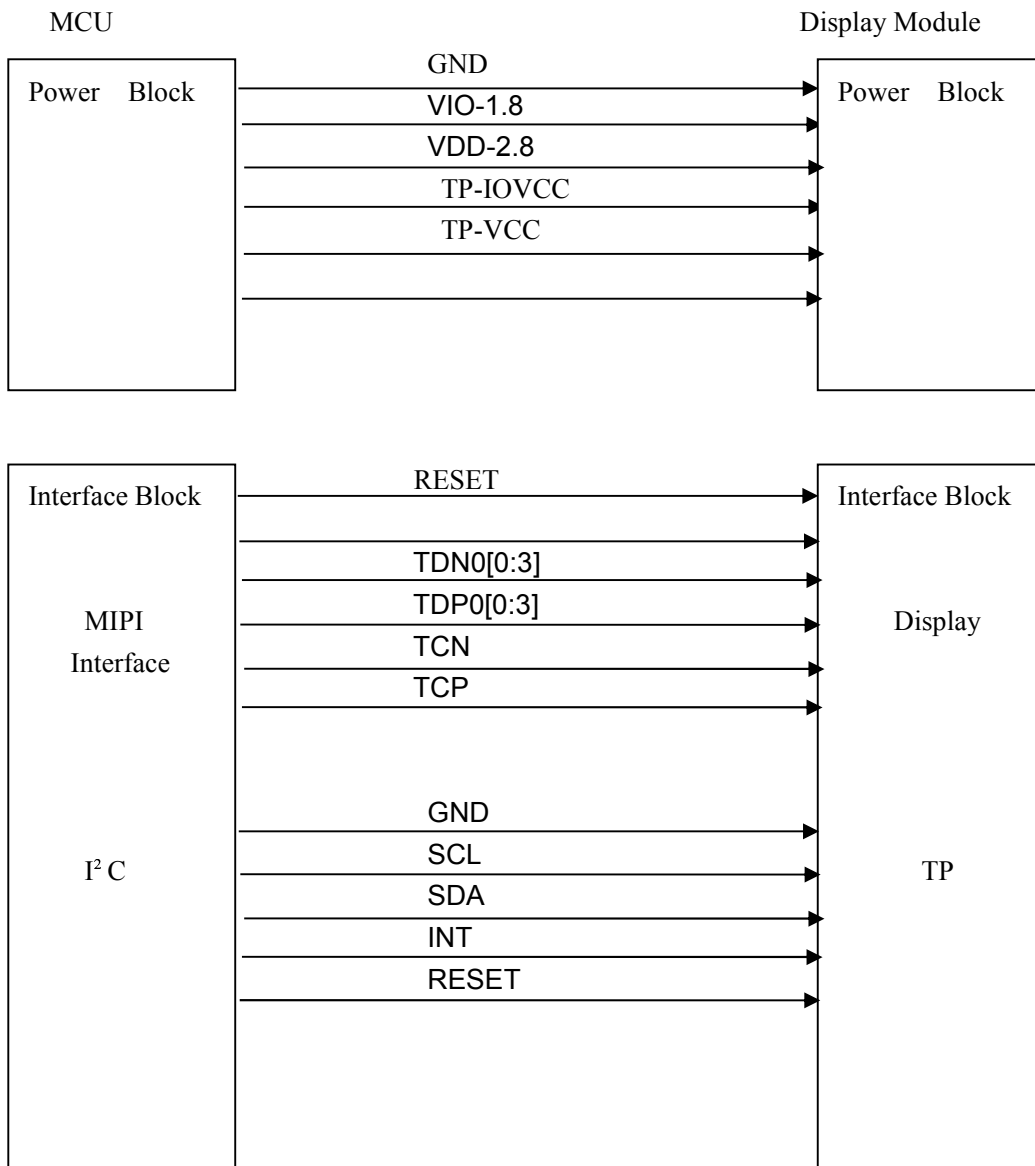
LCM Pin NO.	Symbol	I/O	Description
1	GND	P	Power Ground
2-6	NC	-	NC
7-9	GND	P	Power Ground
10	MTP_PWR		NC
11	TE	I	The signal will reset the LCM, Signal is active low.
12	RESET	I	The signal will reset the LCM, Signal is active low.
13	IOVCC-1.8	P	A power supply for the logic power and I/O circuit(1.8V)
14	GND	P	Power Ground
15	TDP2	I	DSI-D2+ differential data signals for MIPI interface
16	TDN2	I	DSI-D2- differential data signals for MIPI interface
17	GND	P	Power Ground
18	TDP1	I	DSI-D1+ differential data signals for MIPI interface
19	TDN1	I	DSI-D1- differential data signals for MIPI interface
20	GND	P	Power Ground
21	TCP	I	DSI-CLK+ differential clock signals for MIPI interface
22	TCN	I	DSI-CLK- differential clock signals for MIPI interface
23	GND	P	Power Ground
24	TDP0	I	DSI-D0+ differential data signals for MIPI interface
25	TDN0	I	DSI-D0- differential data signals for MIPI interface
26	GND	P	Power Ground
27	TDP3	I	DSI-D3+ differential data signals for MIPI interface
28	TDN3	I	DSI-D3- differential data signals for MIPI interface
29	GND	P	Power Ground
30	VDD-3.3	P	A power supply for the logic power and I/O circuit(3.3V)
31	GND	P	Power Ground
32	TP-VCC 2.8V	P	TP-VCC(2.8V) Power Supply for TP
33	TP-VCC 1.8V	P	TP-VCC(1.8V) Power Supply for TP
34	TP-INT	O	Interrupt signals for TP
35	TP-SDA	I/O	I2C data signals for TP
36	TP-SCL	I	I2C clock signals for TP
37	TP-RST	I	The signal will reset the TP, Signal is active low.
38	NC	-	NC
39	GND	P	Power Ground

I: Input; O: Output; P: Power



3.2 block diagram

MCU and Display Module Interface Configuration





4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ 5.5	V
Power supply voltage	VDDA, VDDB, VDDR, VDDAM, VCC	-0.3 ~ 5.5	V
Supply voltage (MV)	AVDD-AVSS	-0.3 ~ 6.6	V
	AVEE-AVSS	-0.3 ~ -6.6	V
Supply voltage (HV)	VGHR - VGLR	-0.3 ~ 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V

5. ELECTRICAL CHARACTERISTICS

5.1 DC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VDD	Operation Voltage	2.5	3.3	3.6	V	Note 1
	VCC	Operating Voltage	1.65	1.8	3.6	V	Note 1
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1
Logic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 2
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 2
Logic High level Output voltage	VOH	I _{out} = -1 mA	0.8* VDDI	-	VDDI	V	Note 2
Logic Low level Output voltage	VOL	I _{out} = +1 mA	0.0	-	0.2* VDDI	V	Note 2
Logic High level input current (Except MIPI)	I _{IHD}	V _{in} =0~VDDI			1	μA	Note 2
Logic Low level input current (Except MIPI)	I _{ILD}	V _{in} =0~VDDI	-1			μA	Note 2
Logic High level input current (MIPI)	I _{IHD}	V _{in} =0~VDDAM			1	μA	Note 2
Logic Low level input current (MIPI)	I _{ILD}	V _{in} =0~VDDAM	-1			μA	Note 2
AVDD booster voltage	AVDD		4.5		6.5	V	Note 2
AVEE booster voltage	AVEE		-6.5		-4.5	V	Note 2
VCL booster voltage	VCL		-VDDDB		-1.5	V	Note 2
VGH booster voltage	VGH		AVDD +VDD		3xAVDD	V	Note 2
VGL booster voltage	VGL		AVEE -AVDD		2AVEE -AVDD -VDD	V	Note 2
Voltage difference between VGHR and VGLR	VGHL	VGHR-VGLR			25	V	Note 2
Gamma reference voltage	VGMP		2.0		AVDD-0.5	V	Note 2,3
	VGSP		0.0		3.3	V	Note 2,3
Osc	F _{osc}		23	25	27	MHz	
Channel deviation voltage	V _{15V}			5	10	mV	

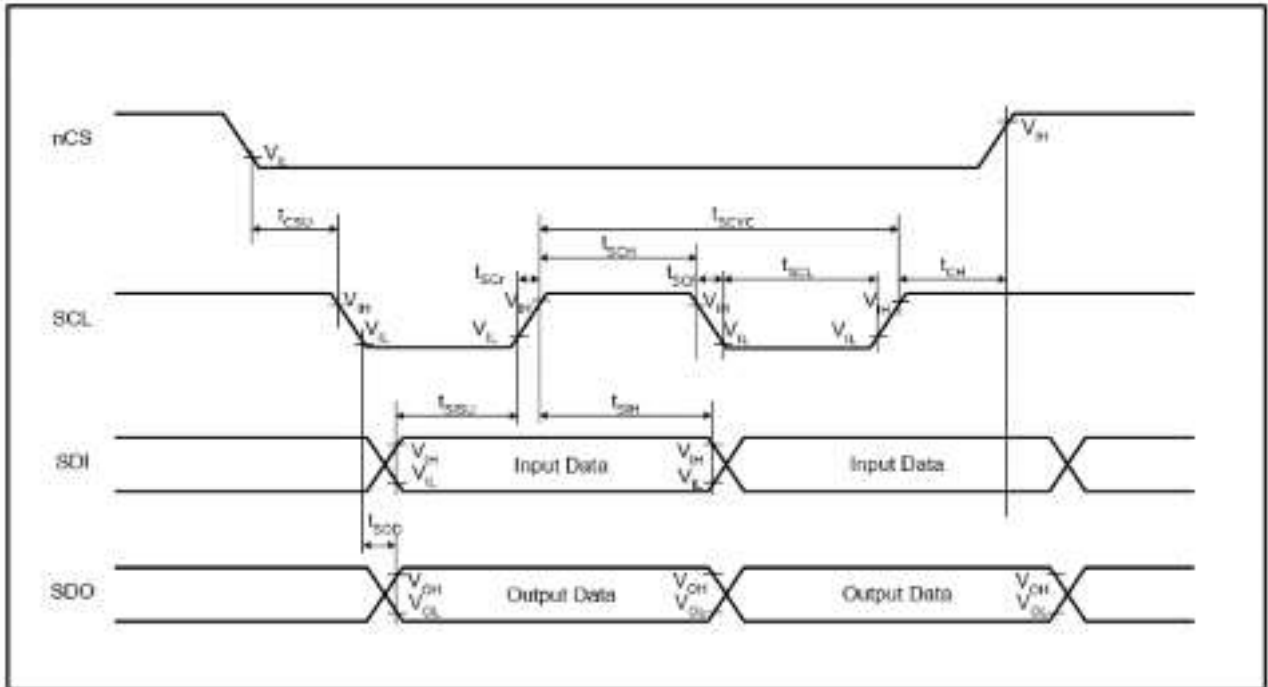
Notes:

1. VDDI=1.65 to 3.3V, VDD=2.5 to 4.8V, VSSI=VSS=VSSS=0V, VDD means VDDA, VDDR, VDDB. And VSS means VSSA, VSSR, VSSB, AVSS, and VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
2. TA = -30 to 85 °C
3. AVDD-0.3V >=VGMP > VGSP



5.2 AC Characteristics

5.31 Serial Interface Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		ns	
	T_{SCYC}	Clock cycle (Read)	300		ns	
	T_{SCH}	Clock "H" pulse width (Write)	40		ns	
	T_{SCH}	Clock "H" pulse width (Read)	140		ns	
	T_{SCL}	Clock "L" pulse width (Write)	40		ns	
	T_{SCL}	Clock "L" pulse width (Read)	140		ns	
	T_{SCR}	Clock rise time		5	ns	
	T_{SCF}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	20		ns	
	T_{CH}	Chip select hold time	50		ns	
SDI	T_{SISV}	Data input setup time	20		ns	
	T_{SIH}	Data input hold time	20		ns	
SDO	T_{SOP}	Data output setup time		120	ns	
	T_{SOH}	Data output hold time	5		ns	

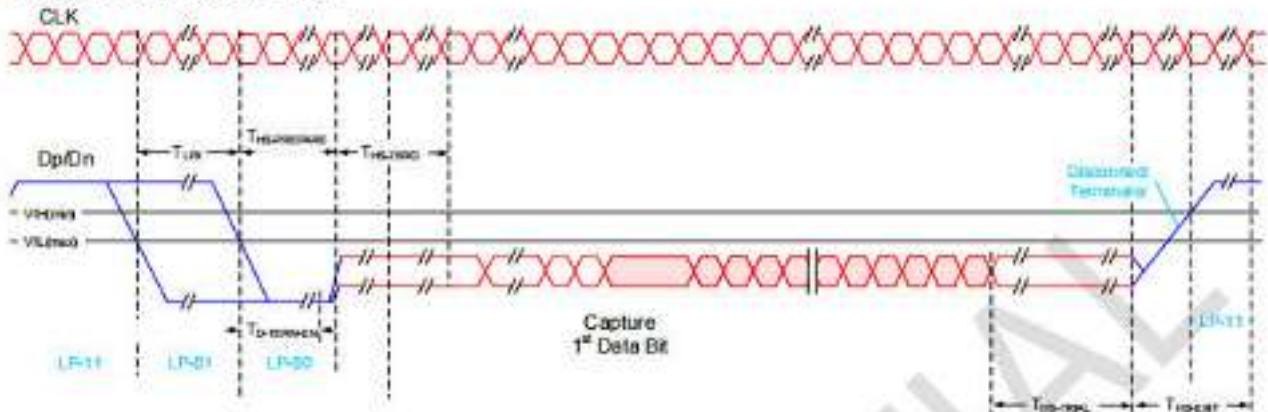
Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: $T_a = -30$ to 70 °C, IOVCC=1.65V to 3.3V, VDD=2.5V to 3.6V, GND=0V

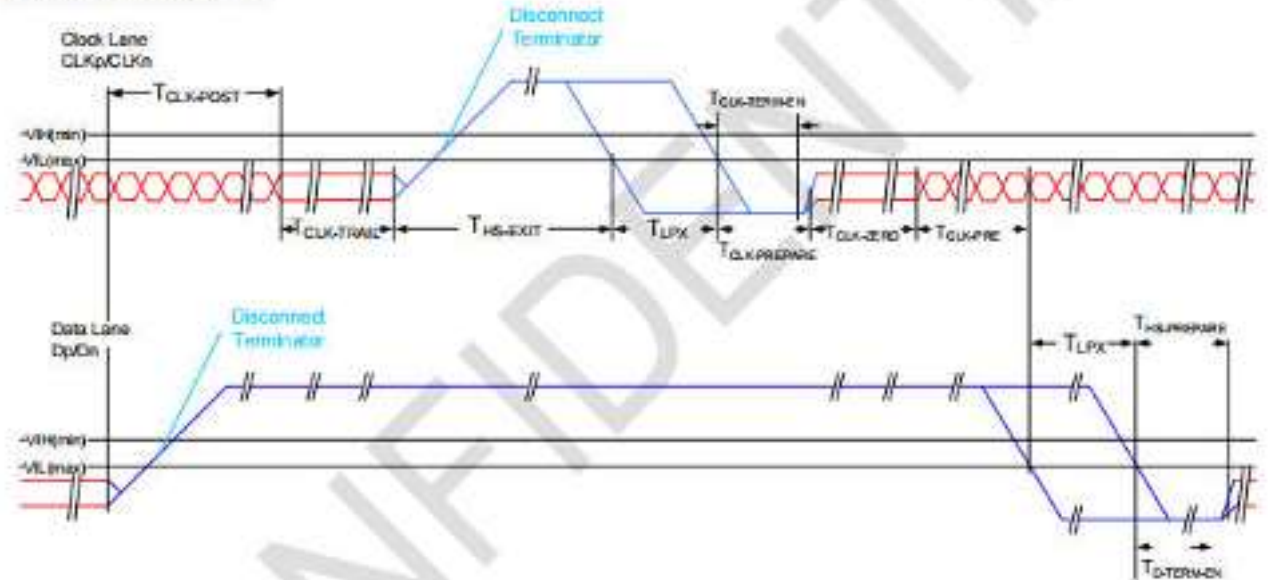


5.32 DSI Timing Characteristics

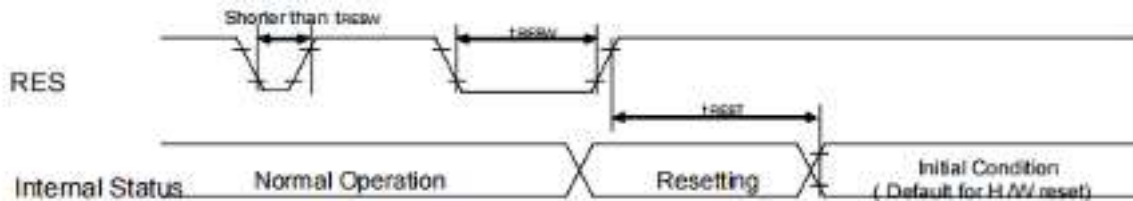
HS Data Transmission Burst



HS dock transmission



5.33 Reset Timing



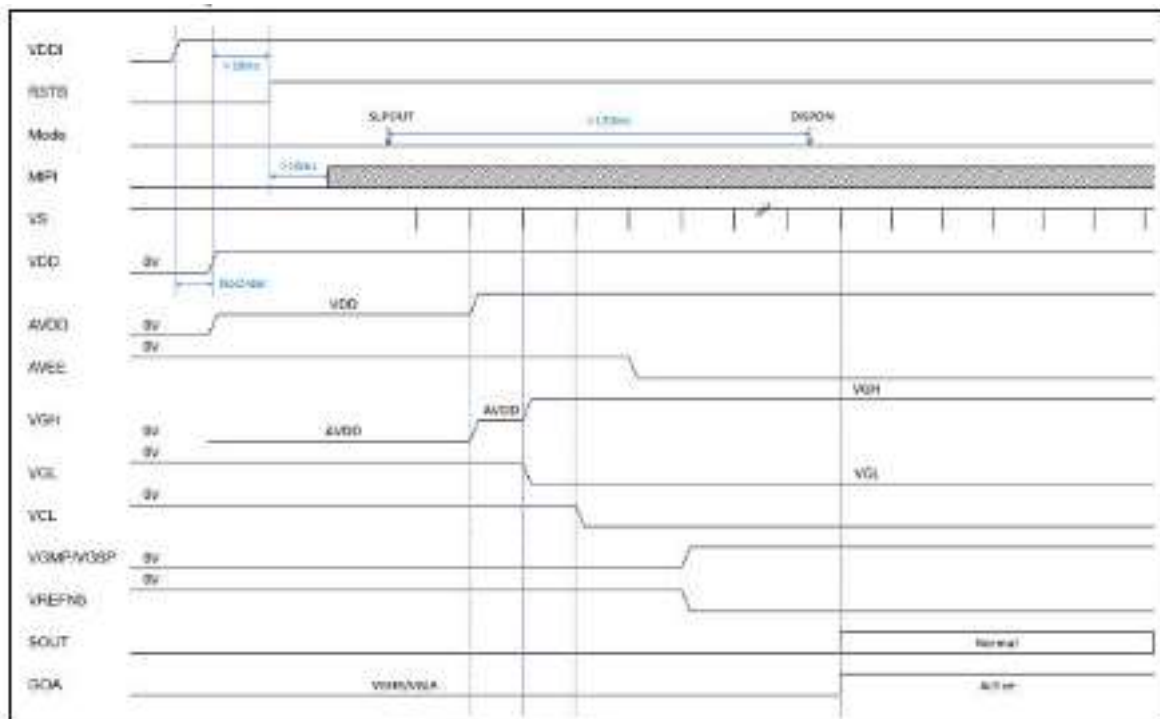
Reset input timing:

IOVCC=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

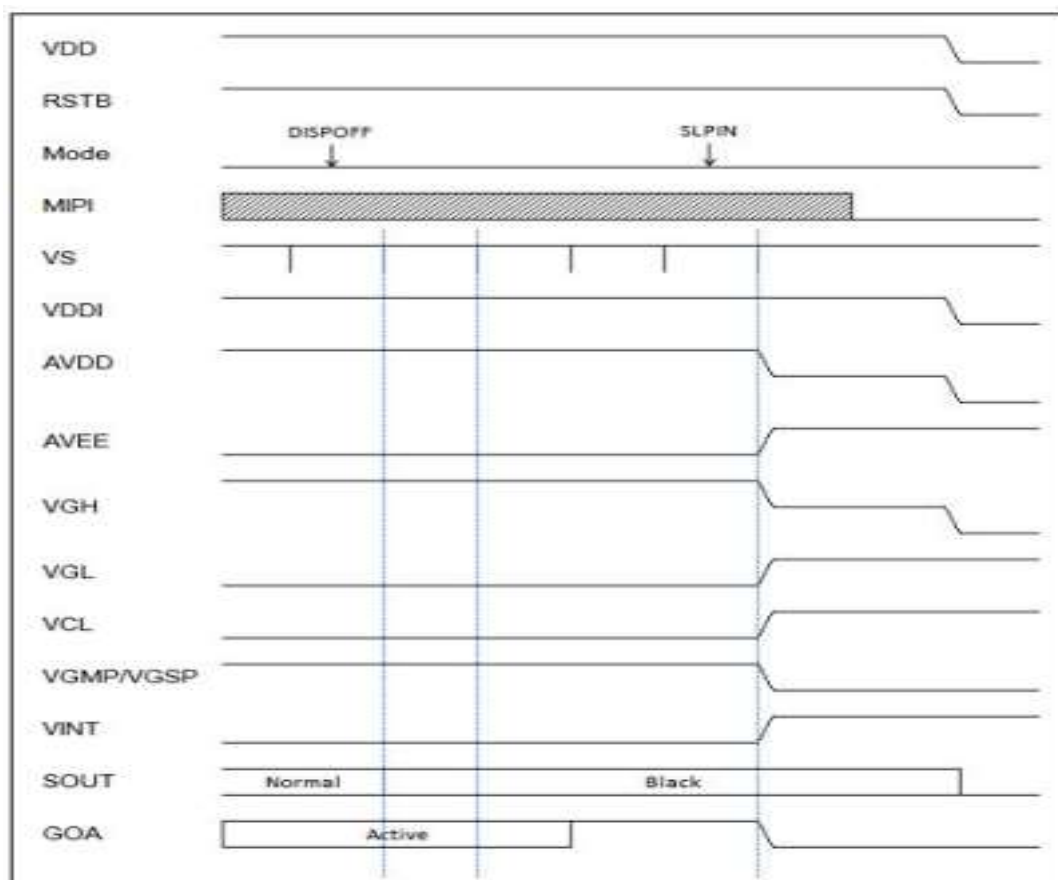
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms



5.4 Power On Sequence



5.5 Power Off Sequence





6. ELECTRO-OPTICAL CHARACTERISTICS

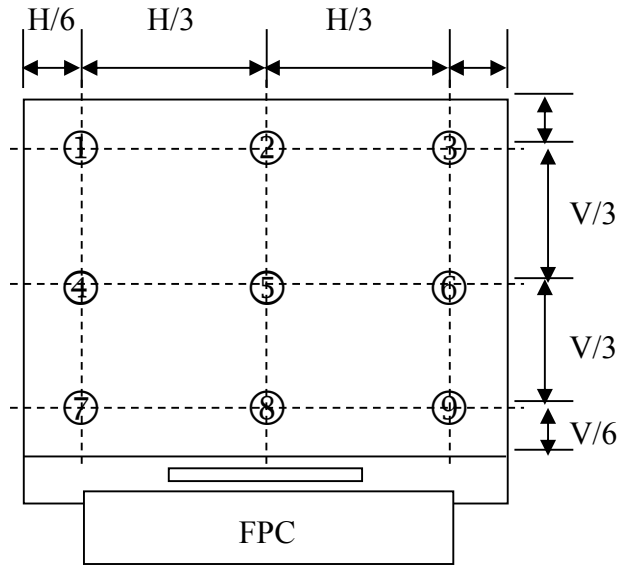
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp	$\Phi_1=0^\circ$	-	320	-	Cd/m ²	1
Uniformity	ΔBp	$\Phi_2=0^\circ$	75%				1,2
Viewing Angle	Φ_1 (up down)	$Cr \geq 10$	80typ			Deg	3
	Φ_2 (left right)		80typ				
Contrast Ratio	Cr	$\Theta=0$ Normal Viewing angle	10000	20000	-	-	4
Response Time			-	-	2	ms	5
Color of CIE Coordinate	W	x	-	-	-	-	1,6
		y	-	-	-	-	
	R	x	-	0.477	-	-	
		y	-	0.528	-	-	
	G	x	-	0.070	-	-	
		y	-	0.578	-	-	
	B	x	-	0.159	-	-	
		y	-	0.146	-	-	



Note1 Definition of Contrast Ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note2: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas (Shown in below), every measuring point is placed at the center of each measuring area.



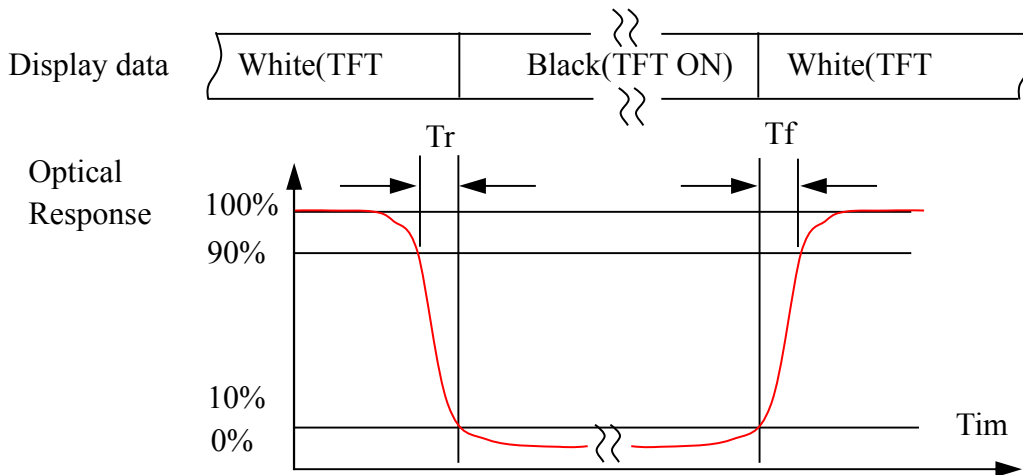
The spot locations for luminance measurement

$$\text{Luminance Uniformity} = \frac{H/6 B_{\min}}{V/6 B_{\max}} \times 100\%$$

B_{\max} : The measured maximum luminance of all measurement position.

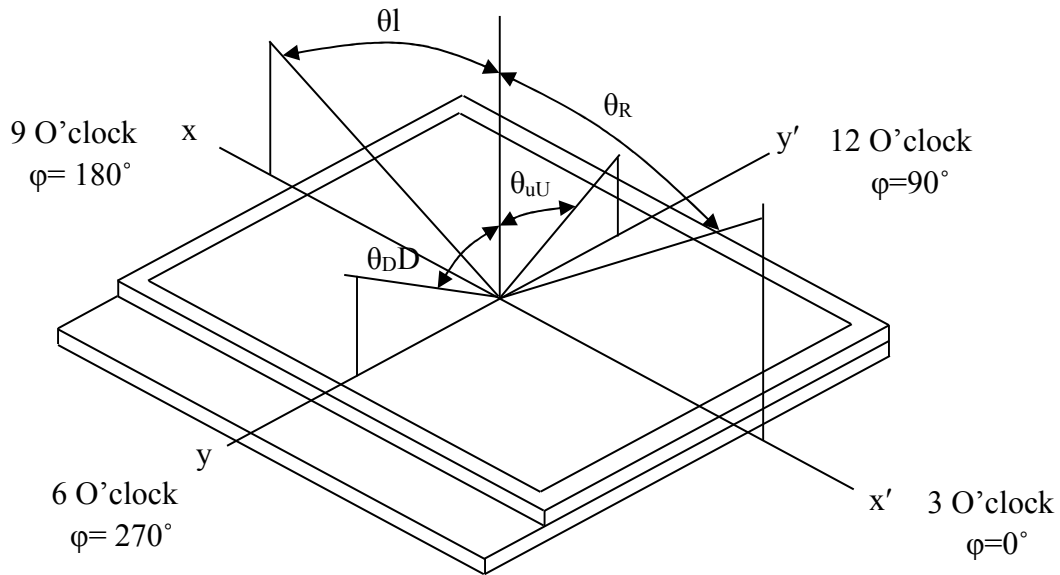
B_{\min} : The measured minimum luminance of all measurement position.

Note 3: Definition of Response time: Sum of T_r and T_f





Note4.Definition of Viewing Angle: The viewing angle range that the $CR \geq 10$



Note 5: Definition of Color Chromaticity (CIE 1931)

Color coordinate of white & red, green, blue at center point.



7. RELIABILITY TEST CONDITIONS

No	Test Item	Test Condition	STANDARD
1	High Temperature Storage	+70°C / 96Hours	1. Functional test is OK. Missing Segment, short, unclear segment, on-display, display abnormally and liquid crystal leak are un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temperature Storage	-55°C / 96Hours	
3	High Temperature Operating	+65°C / 96Hours	
4	Low Temperature Operating	-40°C / 96Hours	
5	Thermal and cold shock	0°C↔+50°C x 10cycles (30min) (5min) (30min)	
6	Operate at High Temperature and Humidity	60°C x 90%RH / 24H	
7	Vibration Test	Frequency: 10Hz~55Hz~10Hz Amplitude:1.5mm, 2 hours for each direction of X, Y, Z	1. Function test is OK. 2. No glass crack, chipped glass, end seal loose and fall, epoxy frame crack and so on. 3. No structure loose and fall.
8	Dropping test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	
9	ESD test	Contact: ±6KV Air: ±10KV 150PF/330Ω,5Points/panel,5times	The test results shall be subject to the whole machine test.

NOTE:

1. The reliability items will be fully performed in new sample qualification,
2. The reliability status will be tested as monitor during mass production. Individual reliability test shall be performed by lot, Moreover, the individual reliability item shall be decided according to reliability plan.
3. All samples are inspected after keeping in the room with normal temperature and humidity for 2 hours or above.
4. Vibration test: It is not necessary to test for those products without assembly frame, backlight, PCB and so on.
5. Dropping test: It is necessary for affirming new package.
6. For the high temperature and high humidity test, pure water of over 10 MΩ.cm should be used.
7. Each test item applies for test LCM only once. Then tested LCM cannot be used again in any other test item.
8. The quantity of LCM examination for each test item is 5pcs to 10pcs.



8. INSPECTION STANDARDS

8.1 AQL Sampling inspection standard

使用 GB/T 2828-2003 一般 II 水平, 采用正常检查一次抽样方式; 具体抽检方式参照《成品检验管理程序》、《抽样管理规范》

缺陷区分	AQL 允收水准
严重缺陷	0 收 1 退
重缺	0.4
轻缺	1.0

8.2 Inspect the condition

8.2.1 在 20—40W 日光灯的照明条件下, 样品离检查者眼睛约 30cm 处进行检查。检验方向以垂直线前后左右 45° (以时钟 3 点、6 点、9 点、12 点)

8.2.2 检验者视力需达到标准视力 1.0 以上。

8.2.3 检验者需戴静电手环、两手八个手指套。

8.2.4 外观检验者以目视检查或以菲林对比卡比对。

8.2.5 电性测试使用电测测架, 主板, 电源线及单片机。

8.2.6 若标准与规格书不符时, 以产品发行之规格书特殊检验规格、工程变更为准

8.2.7 辉色度检测请参照样品, 检测方法依照辉色度检验标准。

8.2.8 电测检验环境: 照度为 200LUX 以下, 外观检验环境: 照度为 600LUX-1000LUX, 检验时间: 1 秒-3 秒。

8.2.9 检验工具: 电测测架, 主板, 电源线及单片机, 菲林对比卡, 游标卡尺, 放大镜, 实体显微镜 (必要时) 等等。

8.3 Judgment criterion

小尺寸点、线判定标准: (6.2 寸以内)

1	点状缺陷 (磨伤、异物、针孔、凹痕、缺膜、气泡、白点、彩点、脏点)		判定 (A/B/C 区)	$D \leq 0.10$, 忽略不计, 但密集型不允许	MI	OK
				$0.1 < D \leq 0.15, ds \geq 10$		$N \leq 2$
				$0.15 < D \leq 0.2, ds \geq 10$		$N \leq 1$
				LCD 亮点: $0.15 < D$		$N \leq 1$
				$D > 0.2$		NG
			判定 (D 区)	同背面丝印油墨区杂质判定标准		
			注: 1) D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下, 判定 OK		MI	
2	线状缺陷 (磨伤、无感划伤、毛屑、纤维等)		判定 (A/B/C 区)	$W \leq 0.03mm, L \leq 3mm, ds \geq 10$	MI	$N \leq 2$
				$0.03mm < W \leq 0.05mm, L \leq 3mm, ds \geq 10$		$N \leq 1$
				$W > 0.05mm$ 或 $L > 3mm$		NG



中尺寸点、线判定标准：（6.2~8寸以内）

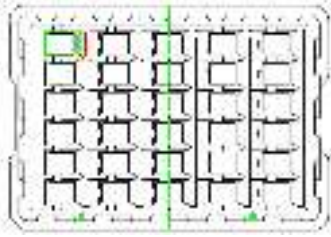
1	点状缺陷 (磨伤、异物、针孔、凹痕、缺膜、气泡、白点、彩点、脏点)		判定(A/B/C区)	$D \leq 0.10$, 忽略不计, 但密集型不允许	MI	OK
				$0.15 < D \leq 0.25$, $ds \geq 10$		$N \leq 2$
				$0.25 < D \leq 3$, $ds \geq 10$		$N \leq 1$
				LCD 亮点: $0.2 < D$		$N \leq 1$
				$D > 0.3$		NG
判定(D区)	同背面丝印油墨区杂质判定标准					
注: 1) D区的点状缺陷需在不影响CTP功能、客户组装及整机的外观的情况下, 判定OK					MI	
2	线状缺陷 (磨伤、无感划伤、毛屑、纤维等)		判定(A/B/C区)	$W \leq 0.03mm$, $L \leq 3mm$, $ds \geq 10$	MI	$N \leq 2$
				$0.03mm < W \leq 0.05mm$, $L \leq 3mm$, $ds \geq 10$		$N \leq 1$
				$W > 0.05mm$ 或 $L > 3mm$		NG

大尺寸点、线判定标准：（8.1~13.3寸以内）

1	点状缺陷 (磨伤、异物、针孔、凹痕、缺膜、气泡、白点、彩点、脏点)		判定(A/B/C区)	$D \leq 0.1$, 忽略不计, 但密集型不允许	MI	OK
				$0.15 < D \leq 0.3$, $ds \geq 10$		$N \leq 2$
				$0.3 < D \leq 0.35$, $ds \geq 10$		$N \leq 1$
				LCD 亮点: $0.25 < D$		$N \leq 1$
				$D > 0.35$		NG
判定(D区)	同背面丝印油墨区杂质判定标准					
注: 1) D区的点状缺陷需在不影响CTP功能、客户组装及整机的外观的情况下, 判定OK					MI	
2	线状缺陷 (磨伤、无感划伤、毛屑、纤维等)		判定(A/B/C区)	$W \leq 0.05mm$, $L \leq 5mm$, $ds \geq 10$	MI	$N \leq 2$
				$0.05mm < W \leq 0.07mm$, $L \leq 5mm$, $ds \geq 10$		$N \leq 1$
				$W > 0.07mm$ 或 $L > 5mm$		NG



9. PACKAGE DRAWING



一盘:TBD pcs

9.2

Use empty tray

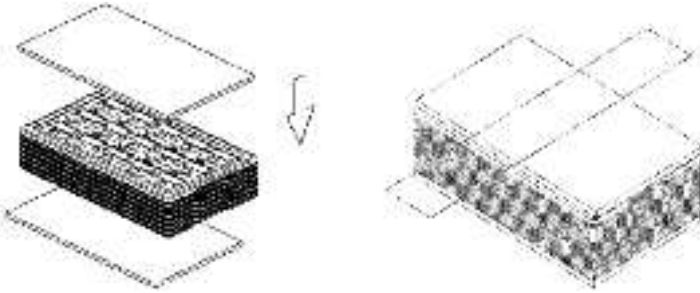


Put products into the tray



一叠:TBD pcs 盘

9.3



9.4

