SPECIFICATION
FOR
TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HL MODEL : HG050FH028T02

☐**Preliminary Specification**

■**Final Specification**

Customer Confirmation column:

Approved by : _____ Dept. : _____ Data : _____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by

Revision History

Version NO.	DATE	Description	Remak
V1.0	2021.10.21	FIRST ISSUE	

CONTENTS

1. GENERAL INFORMATION

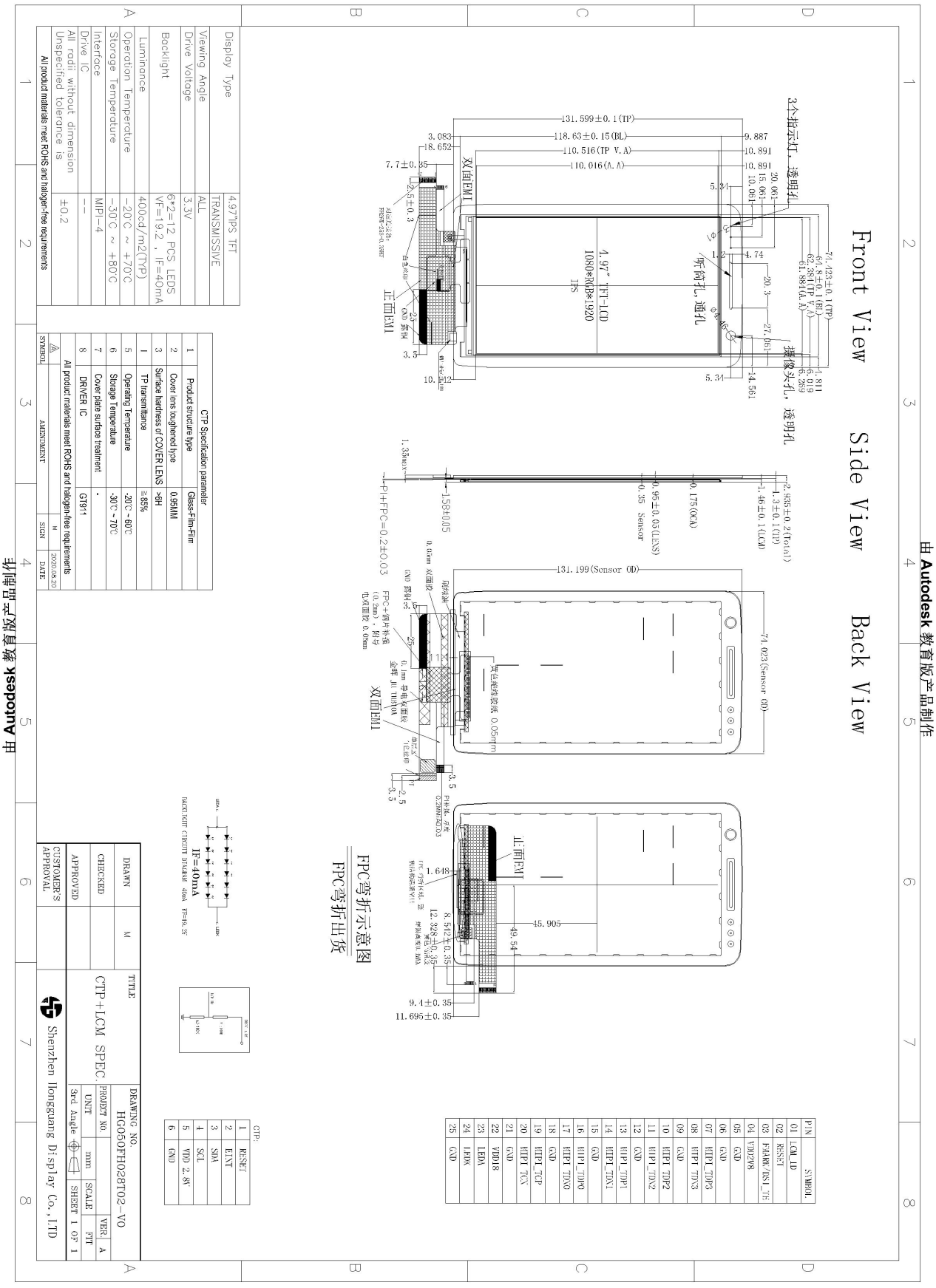
1.1 features

1) Structure: TFT PANNEL+IC+FPC+BL+CTP
2) IPS Type LCD 1080 dot-segment and 1920 dot-common outputs
3) 16.7M Color can be selected by software
4) White LED back light
5) MIPI-4 interface
6) Operation Temperature : -20~70℃
7) Storage Temperature : -30~80℃
8) CTP cover lens : Asahi
9) CTP structure : G+F+F
10) LED life time: -/

1.2 General specification

Item of	Contents	Unit
Panel Size	5.0	inch
LCD Type	a-si/TRANSMISSIVE	/
Display mode	Normally Black	/
Pixel arrangement	1080*3(RGB)*1920	Dots
Pixel pitch (W*H)	0.01905 (H)*RGB*0.05710(V)	um
Active Area	61.641(H)*109.584(V)	Mm
Module area (W*H*T)	74.42(H)*131.6(V)*2.95(T)	Mm
Recommended Viewing Direction	ALL	O’ clock
LCM IC	HX8399C	/
TP IC	GT911	
Interface	MIPI-4	/
Luminance for LCM+TP	350	cd/m2
NTSC	80	%
Weight	TBD	g

2. DIAGRAM FOR LCM



3. I/O CONNECTION & BLOCK DIAGRAM

3.1 I/O connection

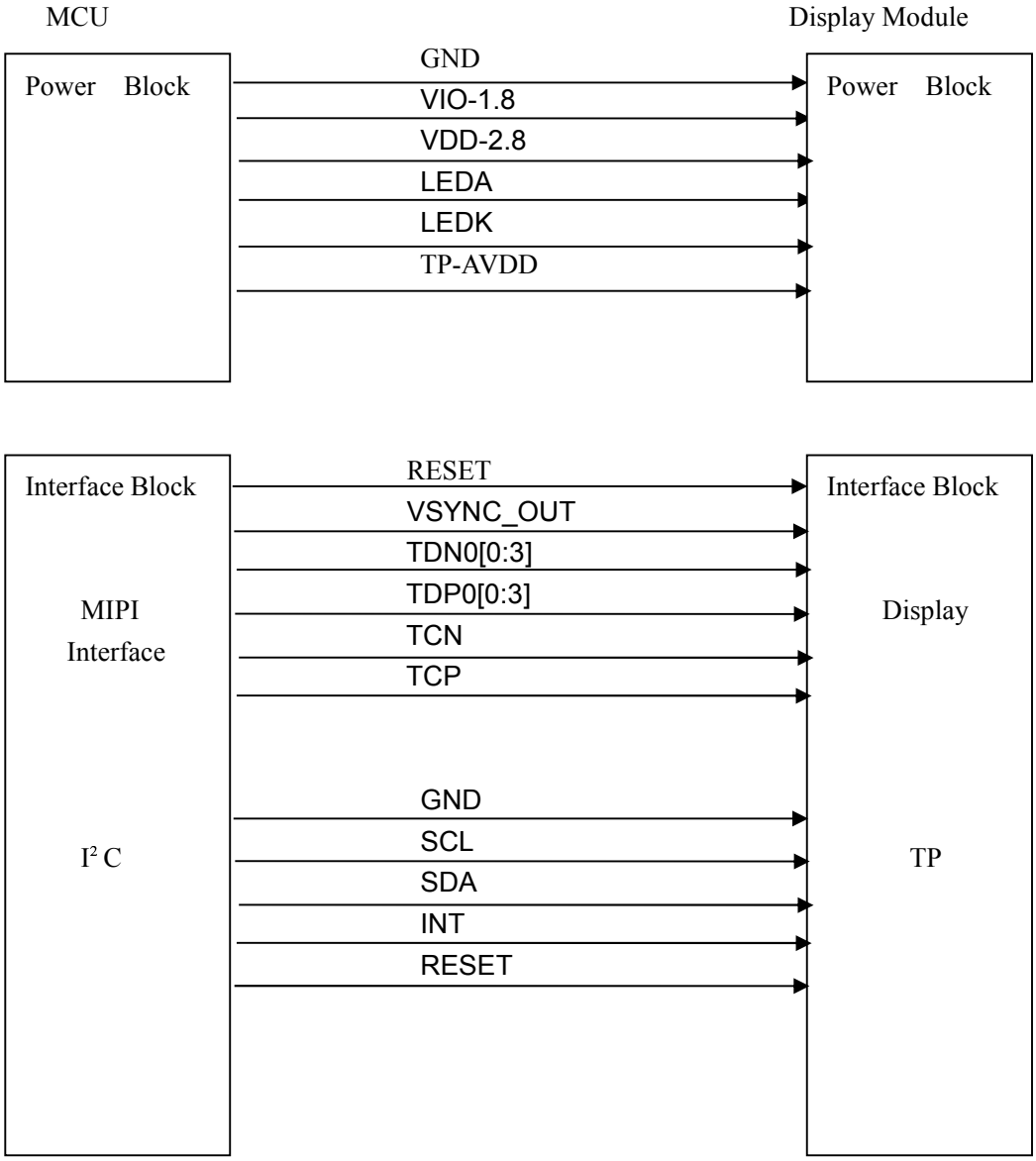
LCM Pin NO.	Symbol	I/O	Description
1	**LCM-ID**	-	ID
2	**RESET**	I	The signal will reset the LCM, Signal is active low.
3	**TE**	-	TE
4	**VDD-2.8**	P	A power supply for the logic power and I/O circuit(2.8V)
5	**GND**	P	Power Ground
6	**GND**	P	Power Ground
7	**TDP3**	I	DSI-D3+ differential data signals for MIPI interface
8	**TDN3**	I	DSI-D3- differential data signals for MIPI interface
9	**GND**	P	Power Ground
10	**TDP2**	I	DSI-D2+ differential data signals for MIPI interface
11	**TDN2**	I	DSI-D2- differential data signals for MIPI interface
12	**GND**	P	Power Ground
13	**TDP1**	I	DSI-D1+ differential data signals for MIPI interface
14	**TDN1**	I	DSI-D1- differential data signals for MIPI interface
15	**GND**	P	Power Ground
16	**TDP0**	I	DSI-D0+ differential data signals for MIPI interface
17	**TDN0**	I	DSI-D0- differential data signals for MIPI interface
18	**GND**	P	Power Ground
19	**TCP**	I	DSI-CLK+ differential clock signals for MIPI interface
20	**TCN**	I	DSI-CLK- differential clock signals for MIPI interface
21	**GND**	P	Power Ground
22	**VDD-1.8**	P	A power supply for the logic power and I/O circuit(1.8V)
23	**LEDA**	P	Power supply for LED anode
24	**LEDK**	P	Power supply for LED cathode
25	**GND**	P	Power Ground

I：Input；O：Output；P：Power

TP Pin NO.	Symbol	I/O	Description
1	**RST**	**I**	The signal will reset the TP, Signal is active low.
2	**INT**	**O**	Interrupt signals for TP
3	**SDA**	**I/O**	I2C data signals for TP
4	**SCL**	**I**	I2C clock signals for TP
5	**AVDD**	**P**	TP-VCC(2.8V) Power Supply for TP
6	**GND**	**P**	Power Ground

3.2 block diagram

MCU and Display Module Interface Configuration



4. ABSOLUTE MAXIMUM RATINGS

(GND=AGND=0V)

Item	Symbol	Values			Unit	Remarks
		Min.	Typ.	Max.		
Power Voltage Supply1	VDD-2.8	2.5	3.3	6.6	V	
Power Voltage Supply2	VIO-1.8	1.65	1.8	3.6	V	
Luminance(LCM+TP)	L_V	-	350	-	cd/m2	
Backlight Forward Voltage	Vf	-	19.2	-	V	
LED Forward Current	If	-	40	-	MA	Note

5. ELECTRICAL CHARACTERISTICS

5.1 LED backlight specification :

项目	符号	额定值	单位
工作电流	I_{BL}	20*2	mA
工作电压	V_{BL}	3.2*6	V
功耗	P_{BL}	768	mW
亮度	Lum	TBD	CD/M^2 (*)
X 色坐标	0.26	0.29	0.32
Y 色坐标	0.27	0.30	0.33

Note:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20Ma(for each led). The LED life time could be decreased if operating $I_L$is larger than 20mA

Note: 12 chips (6 series 2 parallel) connection, LED luminous color: WHITE.

5.2 DC characteristics

(VSP=4.8 to 6V, VSN=-4.8 to -6, VDD1=1.65 to 3.3V, T_A=-40 to 85 °C)

Parameter	Symbol	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
Input high voltage	V_{IH}	VDD1= 1.65 ~ 3.3V	0.7 VDD1	-	VDD1	V
Input low voltage	V_{IL}		0	-	0.3 VDD1	V
VPP	V_{IH} / V_{IL}	VPP	7.25V	7.5V	7.75V	V
Output high voltage (SDO, CABC_PWM_OUT)	V_{OH1}	I_{OH} = -1.0 mA	0.8 VDD1	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT)	V_{OL1}	VDD1= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 VDD1	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	uA
		RESX, DCX, CSX, SCL	-	-	1	uA
	I_{IHD}	DB[7...0], SDI_SDA, DCX	-	-	1	uA
		DB[7...0]	-	-	1	uA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-	-	uA
		RESX, DCX, CSX, SCL	-1	-	-	uA
	I_{ILD}	DB[7...0], SDI_SDA, DCX	-1	-	-	uA
		DB[7...0]	-1	-	-	uA
Current consumption Sleep in mode (VSP-VSSA)	$I_{ST(VSP)}$	VDD3=2.8V, VDD1=1.8V, HS_VCC T_A=25°C	-	-	TBD	uA
Current consumption Sleep in mode (VSN-VSSA)	$I_{ST(VSN)}$		-	-	TBD	uA
Current consumption Sleep in mode (VDD1– VSSD)	$I_{ST(VDD1)}$		-	-	TBD	uA
Current consumption Sleep in mode (HS_VCC– HS_VSS)	$I_{ST(HS\_VCC)}$		-	-	TBD	uA
Current consumption Deep Sleep in mode (VSP-VSSA)	$I_{DST(VSP)}$		-	-	TBD	uA
Current consumption Deep Sleep in mode (VSN-VSSA)	$I_{DST(VSN)}$		-	-	TBD	uA
Current consumption Deep Sleep in mode (VDD1– VSSD)	$I_{DST(VDD1)}$		-	-	TBD	uA
Current consumption Deep Sleep in mode (HS_VCC– HS_VSS)	$I_{DST(HS\_VCC)}$		-	-	TBD	uA

5.2.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: High-Speed Receiver **(HS-RX)**, Low Power Transmitter **(LP-TX)**, a Low-Power Receiver **(LP-RX)**, and the Low-Power Contention Detector **(LP-CD)**. Figure 8.3 shows the complete set of electrical functions required for a fully featured PHY transceiver.

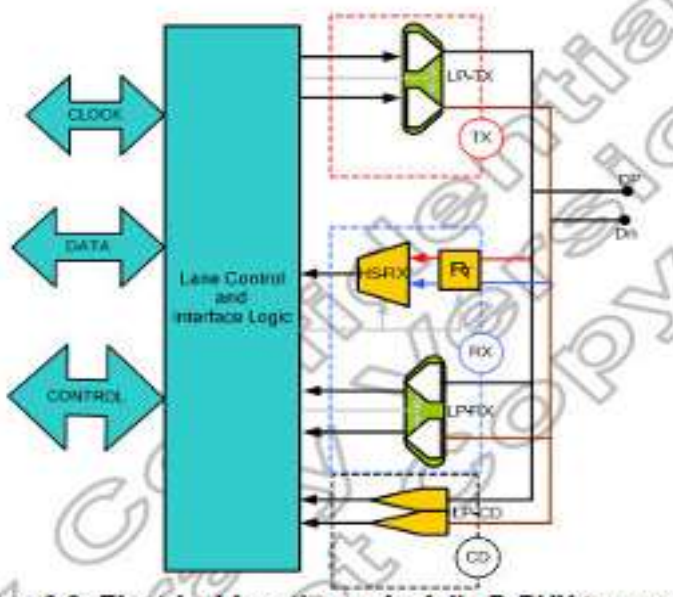


Figure 8.3: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.4 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

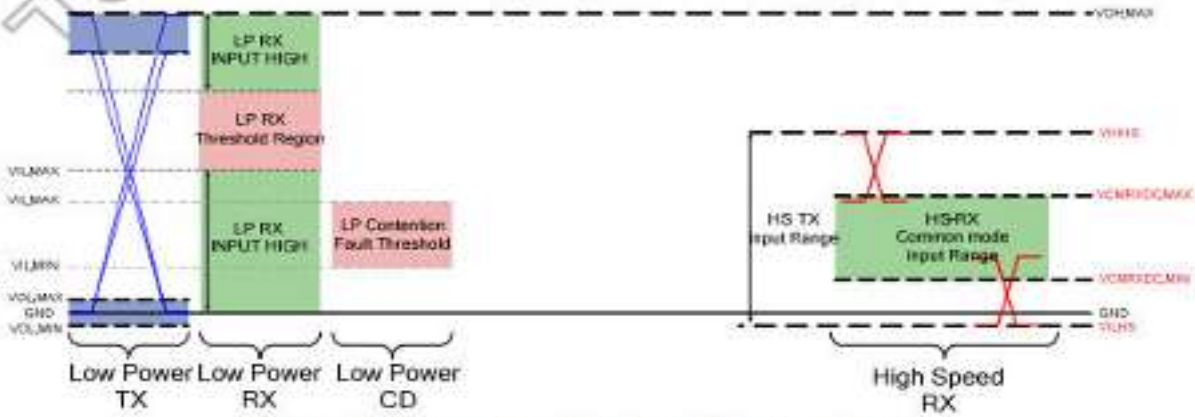


Figure 8.4: Shows both the HS and LP signal levels

5.2.2 DC Characteristics for CTP

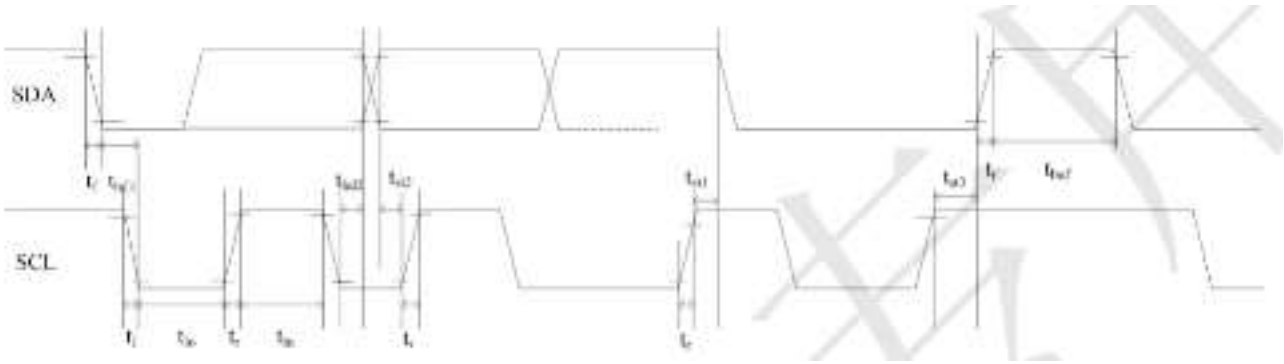
(Ta = 25 °C, TP_VDD=2.8V, TP_IOVCC1.8V=1.8V or TP-VDD=TP_VDD2.8V

Item	Symbol	Min.	Typ.	Max.	Unit
Logic High level input voltage	VIH	0.75*TP_VDD2.8V	-	TP_ VDD2.8V +0.3	V
Logic Low level input voltage	VIL	-0.3	-	0.25* TP_ VDD2.8V	V
Logic High level output voltage	VOH	0.85*TP_VDD2.8V	-	-	V
Logic Low level output voltage	VOL	-	-	0.15* TP_ VDD2.8V	V

5.3 TP_AC Characteristics

5.3.1 I2C interface timings

High Speed Data Transmission: Data-Clock Timing



Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Note:通讯接口 3.3V 通讯接口，400Kbps 通讯速度，上拉电阻 2K

5.4 AC Characteristics

5.4.1 High Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR **(half-rate)** clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrate phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CP – CN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.6.

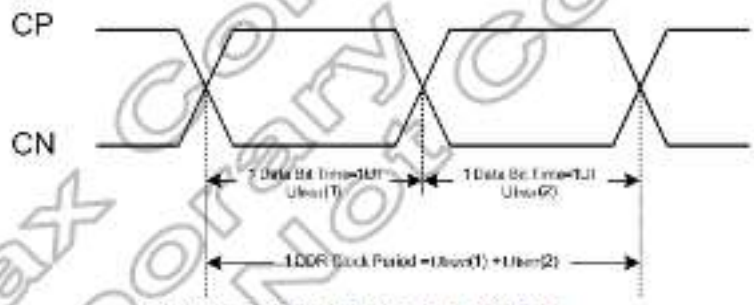


Figure 8.7: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.12.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous[1,2,3]	UI_{INST}	-	-	12.5	ns

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 4Gbps of 4 data lanes 24-bit data format/ 3Gbps of 4 data lane 18-bit data format/ 2.67Gbps of 4 data lane 16-bit data format.

Table 8.12: Re verse HS data transmission timing parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.7. Data is launched in a quadrate relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

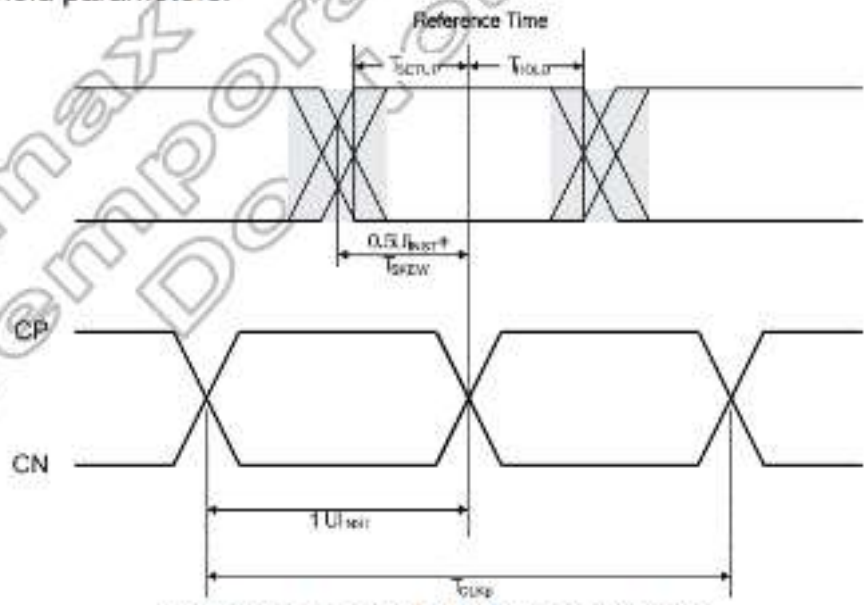


Figure 8.8: Data to clock timing definitions

5.4.2 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.13. Implementers shall specify a value UIINST, MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.13 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrate clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*UIINST, i.e. ±0.2*UIINST for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UI_{INST}.
(2) 0.15UI is only for reference, related to the signal jitter caused by the transmittion path, this spec need to check on panel performance to fine tune.

Table 8.13: Data to clock timing specifications

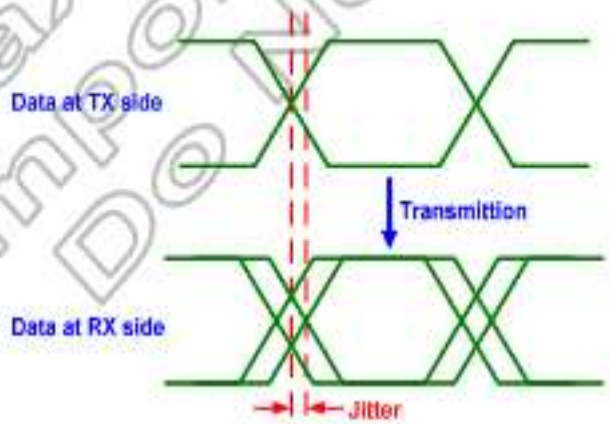
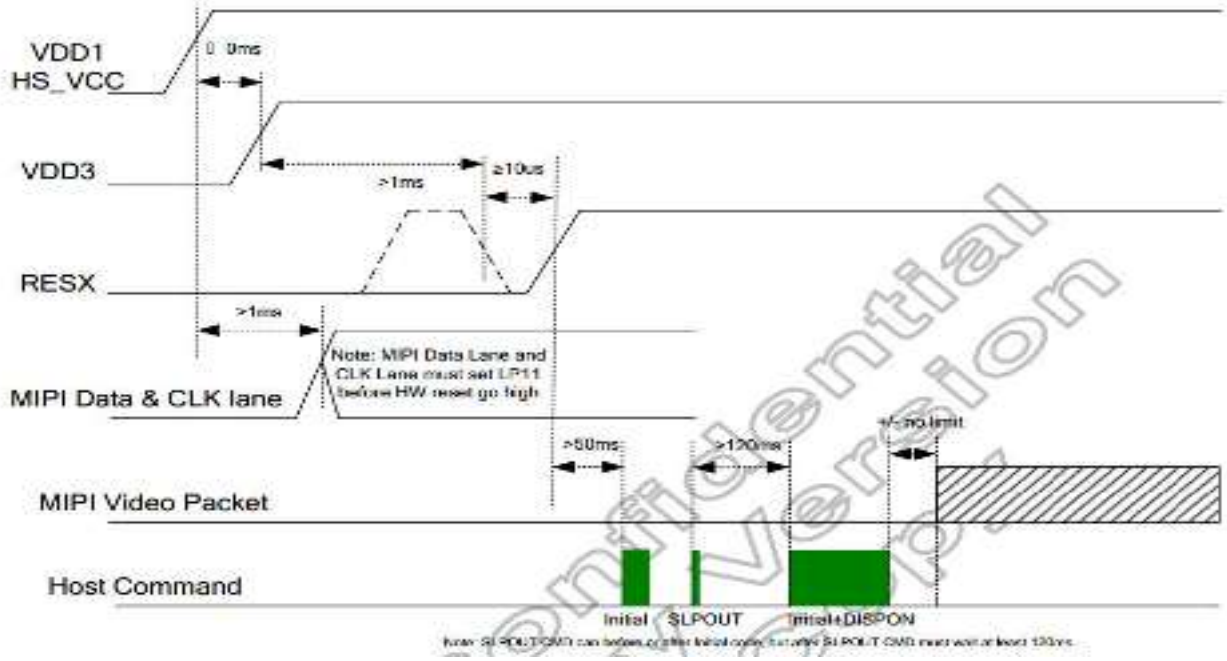


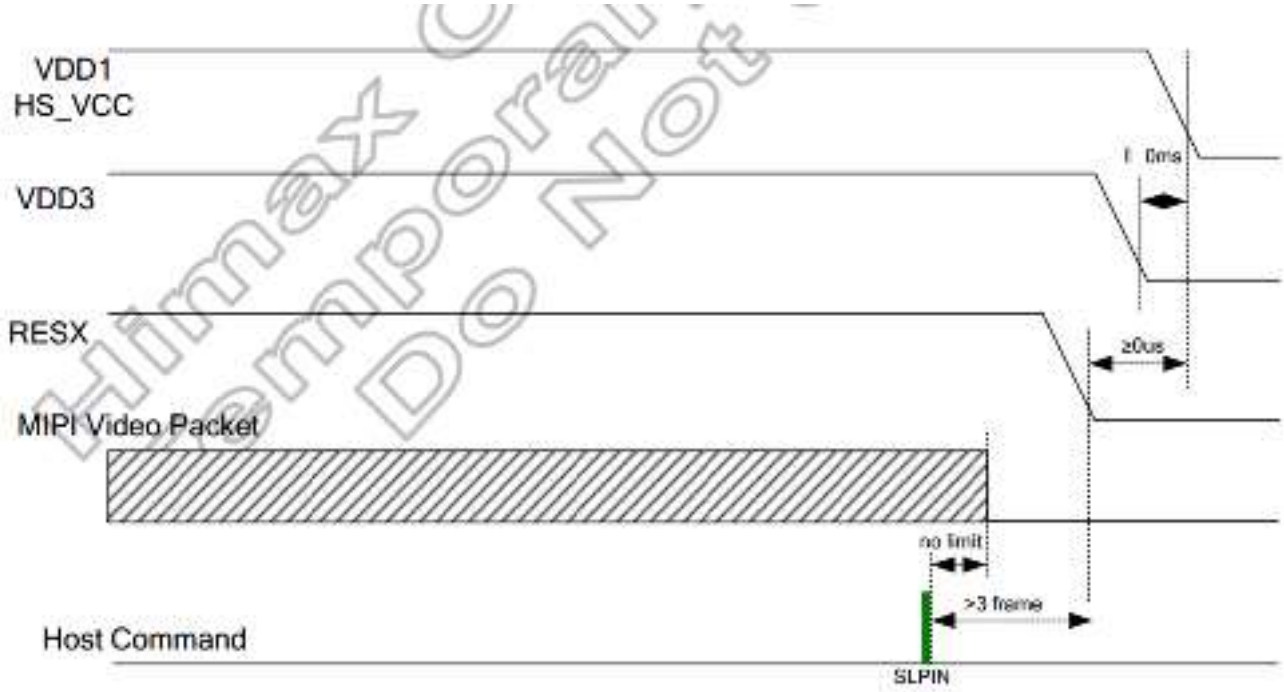
Figure 8.9: Skew window of transmittor and receiver

5.5 Power ON/OFF Sequence 电源开关序列

5.5.1 VDD3/VDD1 input power on sequence



5.5.2 VDD3/VDD1 input power off sequence



5.6 Reset Timing

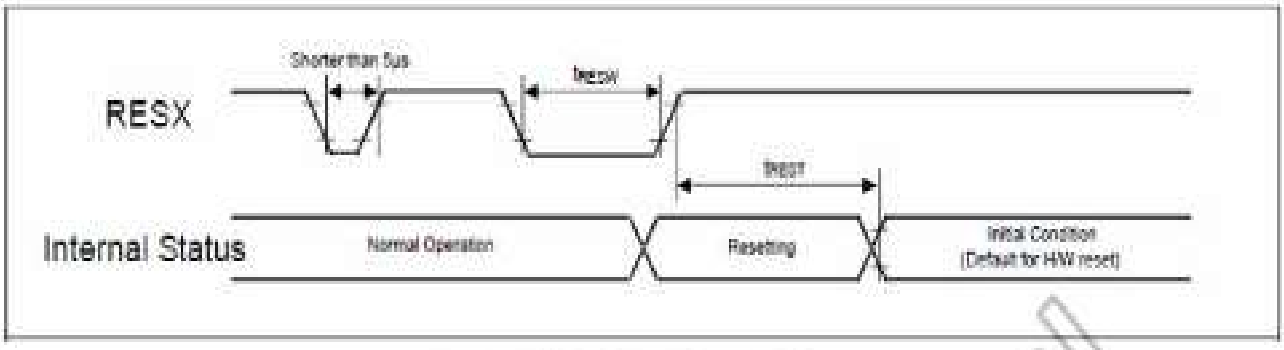


Figure 8.12: Reset input timing

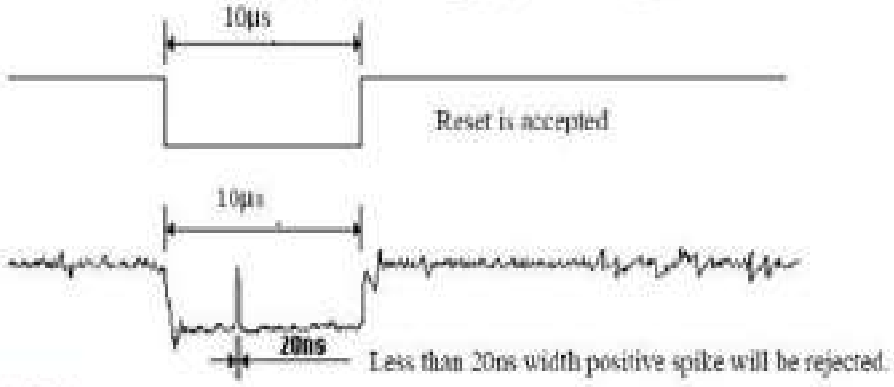
Symbol	Parameter	Related pins	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Note
t_{RESW}	Reset low pulse width[1]	RESX	10	-	-	μs	-
t_{REST}	Reset complete time[2]	-	-	-	50	ms	-

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 50ms after a rising edge of RESX.

(3) Spike Rejection also applies during a valid reset pulse as shown below.



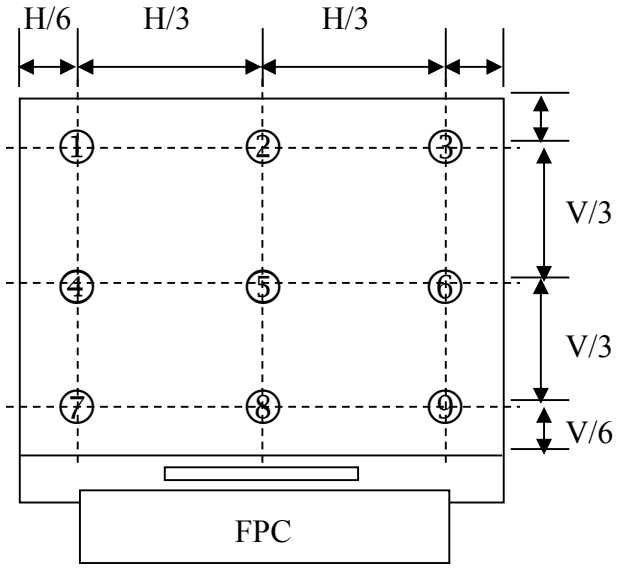
6. ELECTRO-OPTICAL CHARACTERISTICS

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		$\Phi_1=0°$ $\Phi_2=0°$	-	350	-	Cd/m^2	1
Uniformity	△Bp			80%				1,2
Viewing Angle	Φ_1(up down)		Cr≥10	80typ			Deg	3
	Φ_2(left right)			80typ				
Contrast Ratio	Cr		Θ=0 Normal Viewing angle	1000	-	-	-	4
Response Time	$Tr+T_f$			-	-	35	ms	5
Color of CIE Coordinate	W	x	$\Phi_1=0°$ $\Phi_2=0°$	-0.02	0.295	+0.02	-	1,6
		y			0.323		-	
	R	x			0.632		-	
		y			0.313		-	
	G	x			0.302		-	
		y			0.579		-	
	B	x			0.143		-	
		y			0.137		-	

Note1 Definition of Contrast Ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note2: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas (Shown in below), every measuring point is placed at the center of each measuring area.



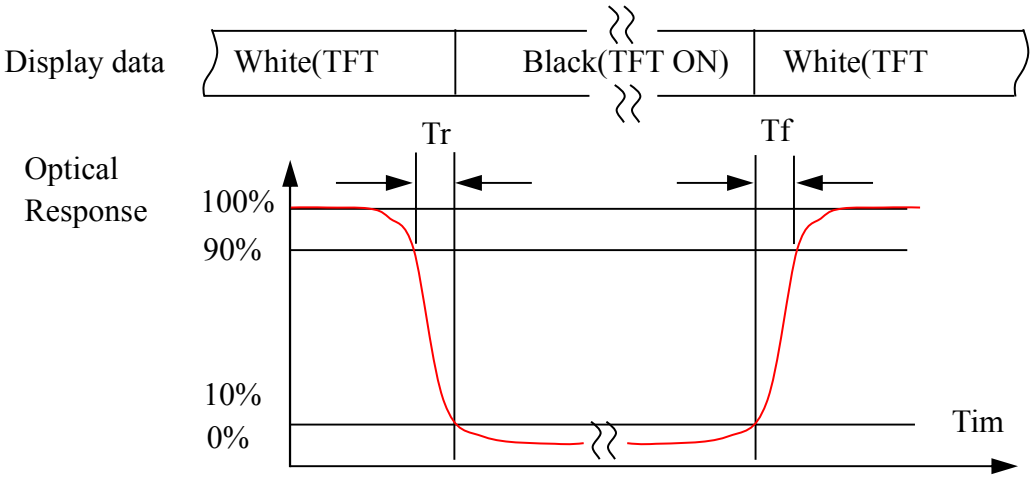
The spot locations for luminance measurement

$$\text{Luminance Uniformity} = \frac{H/6\ B_{min}}{V/6\ B_{max}} \text{x100\%}$$

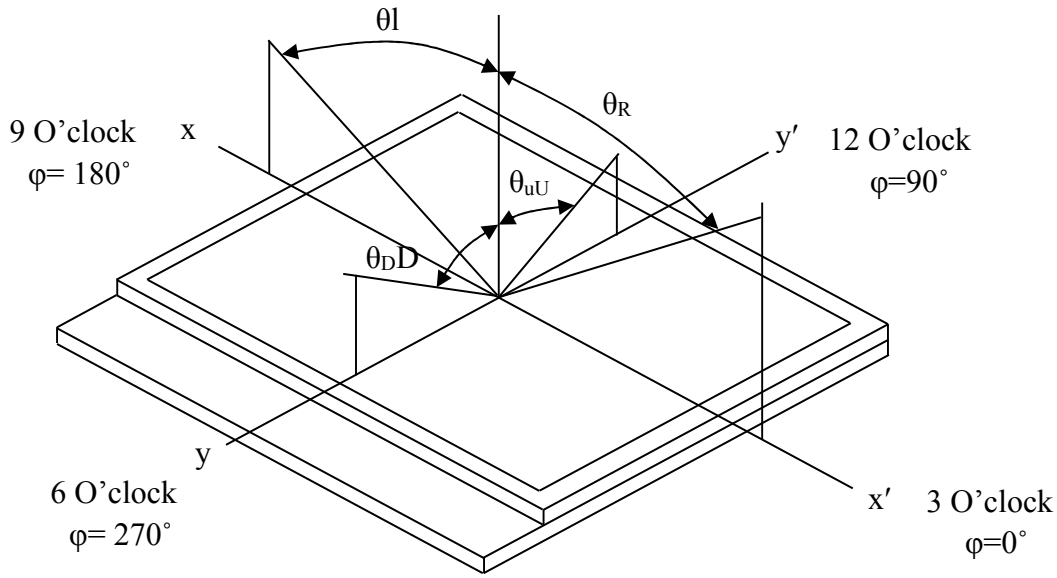
B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

Note 3:Definition of Response time: Sum of Tr and Tf



Note4.Definition of Viewing Angle: The viewing angle range that the CR≥10



Note 5: Definition of Color Chromaticity (CIE 1931)

Color coordinate of white & red, green, blue at center point.

7. RELIABILITY TEST CONDITIONS

No	Test Item	Test Condition	STANDARD
1	High Temperature Storage	+80°C / 96Hours	1. Functional test is OK. Missing Segment, short, unclear segment, on-display, display abnormally and liquid crystal leak are un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temperature Storage	-30°C / 96Hours	
3	High Temperature Operating	+70°C / 96Hours	
4	Low Temperature Operating	-20°C / 96Hours	
5	Thermal and cold shock	0°C⇆+50°C x 10cycles (30min) (5min) (30min)	
6	Operate at High Temperature and Humidity	60°C x 90%RH / 24H	
7	Vibration Test	Frequency: 10Hz~55Hz~10Hz Amplitude:1.5mm, 2 hours for each direction of X, Y, Z	1. Function test is OK. 2. No glass crack, chipped glass, end seal loose and fall, epoxy frame crack and so on. 3. No structure loose and fall.
8	Dropping test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	
9	ESD test	Contact: ±6KV Air: ±10KV 150PF/330Ω,5Points/panel,5times	The test results shall be subject to the whole machine test.

NOTE:

1. The reliability items will be fully performed in new sample qualification,
2. The reliability status will be tested as monitor during mass production. Individual reliability test shall be performed by lot , Moreover, the individual reliability item shall be decided according to reliability plan.
3. All samples are inspected after keeping in the room with normal temperature and humidity for 2 hours or above.
4. Vibration test: It is not necessary to test for those products without assembly frame , backlight , PCB and so on.
5. Dropping test : It is necessary for affirming new package.
6. For the high temperature and high humidity test, pure water of over 10 MΩ.cm should be used.
7. Each test item applies for test LCM only once . Then tested LCM cannot be used again in any other test item.
8. The quantity of LCM examination for each test item is 5pcs to 10pcs.

8. INSPECTION STANDARDS

8.1 AQL Sampling inspection standard

使用 GB/T 2828-2003 一般 II 水平,采用正常检查一次抽样方式；具体抽检方式参照《成品检验管理程序》、《抽样管理规范》

缺陷区分	AQL 允收水准
严重缺陷	0 收 1 退
重缺	0.4
轻缺	1.0

8.2 Inspect the condition

8.2.1 在 20—40W 日光灯的照明条件下，样品离检查者眼睛约 30cm 处进行检查。检验方向以垂直线前后左右 45°（以时钟 3 点、6 点、9 点、12 点）

8.2.2 检验者视力需达到标准视力 1.0 以上。

8.2.3 检验者需戴静电手环、两手八个手指套。

8.2.4 外观检验者以目视检查或以菲林对比卡比对。

8.2.5 电性测试使用电测测架,主板,电源线及单片机。

8.2.6 若标准与规格书不符时，以产品发行之规格书特殊检验规格、工程变更为准

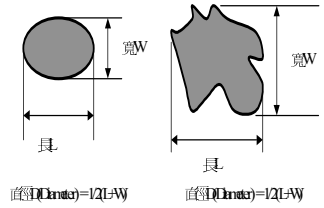
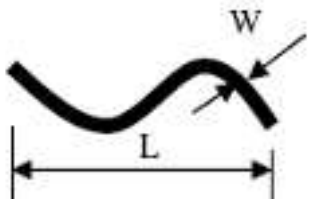
8.2.7 辉色度检测请参照样品,检测方法依照辉色度检验标准。

8.2.8 电测检验环境:照度为 200LUX 以下,外观检验环境：照度为 600LUX-1000LUX，检验时间：1 秒-3 秒。

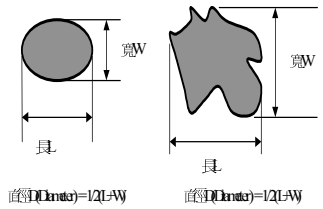
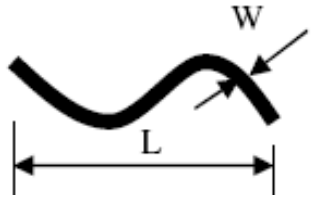
8.2.9 检验工具:电测测架,主板,电源线及单片机,菲林对比卡,游标卡尺,放大镜,实体显微镜(必要时)等等。

8.3 Judgment criterion

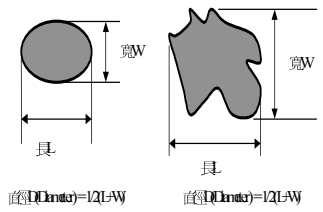
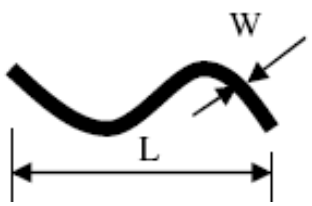
小尺寸点、线判定标准：（6.2 寸以内）

1	点状缺陷（磨伤、异物、针孔、凹痕、缺膜、气泡，白点、彩点、脏点）		判定（A/B/C 区）	*D≤0.10,忽略不计,但密集型不允许*	MI	OK
				0.1<D≤0.15，ds≥10		N≤2
				0.15<D≤0.2，ds≥10		N≤1
				LCD 亮点：0.15<D		N≤1
				D>0.2		NG
			判定（D 区）	同背面丝印油墨区杂质判定标准		
			注：1）D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下，判定 OK		MI	
2	线状缺陷（磨伤、无感划伤、毛屑、纤维等）		判定（A/B/C 区）	*W≤0.03mm，L≤3mmm，ds≥10*	MI	N≤2
				0.03mm<W≤0.05mm，L≤3mm，ds≥10		N≤1
				W>0.05mm 或 L>3mm		NG

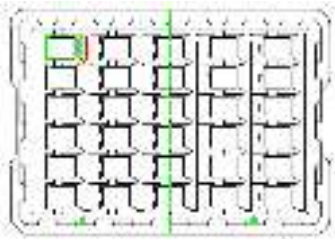
中尺寸点、线判定标准：（6.2~8 寸以内）

1	点状缺陷（磨伤、异物、针孔、凹痕、缺膜、气泡，白点、彩点、脏点）		判定（A/B/C 区）	*D≤0.10，忽略不计，但密集型不允许*	MI	OK
				0.15<D≤0.25，ds≥10		N≤2
				0.25<D≤3，ds≥10		N≤1
				LCD 亮点：0.2<D		N≤1
				D>0.3		NG
			判定（D 区）	同背面丝印油墨区杂质判定标准		
			注：1）D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下，判定 OK		MI	
2	线状缺陷（磨伤、无感划伤、毛屑、纤维等）		判定（A/B/C 区）	*W≤0.03mm，L≤3mmm，ds≥10*	MI	N≤2
				0.03mm<W≤0.05mm，L≤3mm，ds≥10		N≤1
				W>0.05mm 或 L>3mm		NG

大尺寸点、线判定标准：（8.1~13.3 寸以内）

1	点状缺陷（磨伤、异物、针孔、凹痕、缺膜、气泡，白点、彩点、脏点）		判定（A/B/C 区）	*D≤0.1，忽略不计，但密集型不允许*	MI	OK
				0.15<D≤0.3，ds≥10		N≤2
				0.3<D≤0.35，ds≥10		N≤1
				LCD 亮点：0.25<D		N≤1
				D>0.35		NG
			判定（D 区）	同背面丝印油墨区杂质判定标准		
			注：1）D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下，判定 OK		MI	
2	线状缺陷（磨伤、无感划伤、毛屑、纤维等）		判定（A/B/C 区）	*W≤0.05mm，L≤5mmm，ds≥10*	MI	N≤2
				0.05mm<W≤0.07mm，L≤5mm，ds≥10		N≤1
				W>0.07mm 或 L>5mm		NG

9. PACKAGE DRAWING

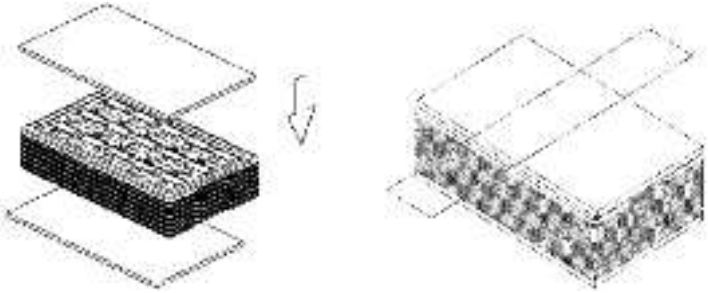


一盘:TBD pcs

9.2

一叠:TBD pcs 盘

9.3



9.4