SPECIFICATION

FOR

TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HL MODEL : HG024QG002

☐ **Preliminary Specification**

■ **Final Specification**

Customer Confirmation column:

Approved by :_____ Dept. :_____ Data :_____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by

Revision History

Rev.	ECN No.	Description of Change	Date	Prepared
01	-	Initial Issue	2022/12/7	
02	-			
	-			

目录

1 Module basic Specification

1.1 Module application

- **This module has a 2.4 inch diagonally measured active area with 450RGBx600 resolutions (600 horizontal by 450 vertical pixel arrays). Each pixel is divided into RED, GREEN, BLUE dots.**
- **This module is display terminals for sports camera and smart home.**

1.2 Display Module Specification

1.2.1 Display Module specification

No	Display Module specification	Support (Y/N)	Remarks
Display	Gamma Correction, RGB Separate γ Correction Function	Y	
	PCD(Panel Crack Detection)	N	
	Command mode	Y	
	Video mode	N	
	Display module brightness value OTP in Register	Y	
	Brightness Dimming	Y	
	AOD（Always On Display）	Y	
	AOD RTC (Always On Display Real_Time Clock)	N	
	CGM(Color Gamut Mapping)	N	

1.2.2 Display Panel specification

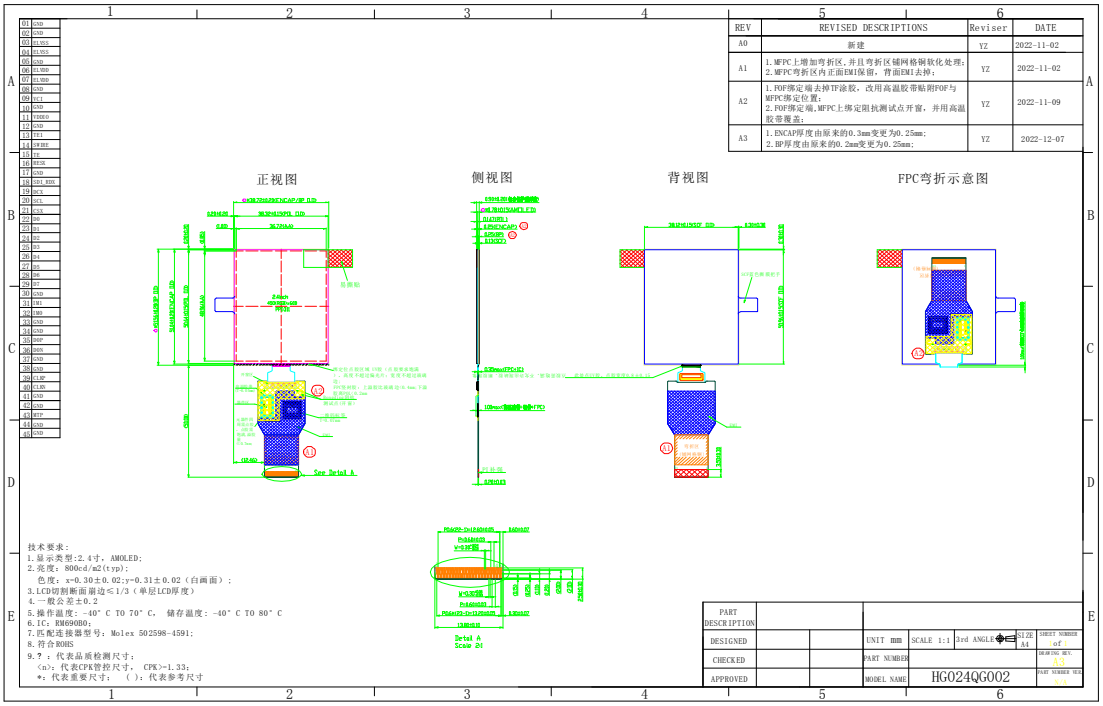
No	Item	Specification	Unit	Remarks
1	Display type	Rigid AMOLED		
2	Display Size	2.4”	Inch	
3	Active Area	36.72*48.96	mm	
4	Panel outline(H x V)	38.72*51.56	mm	
5	Pixel Size	81.6 x 81.6	um	
6	Pixel Pitch	81.6	um	
7	Pixel Per inch	311	PPI	

8	Resolution	450RGB*600		
9	Color Depth	16.7M(24bit)		
10	Viewing Direction	All direction		
11	Pixel Aspect Ratio	3:4		
12	Frame rate	60	Hz	
13	Drive mux	1:6		
14	Driver IC (Type)	RM690B0		
15	Driver IC/ RAM Size	1/3RAM		
16	Panel bonding type	COF		
17	Interface	SPI/MCU/MIPI		
18	TFT Technology Type	LTPS		
19	Encap glass height	0.25	mm	
20	TFT glass height	0.25	mm	
21	Frit glue width	≥0.4	mm	
22	Panel gate scan direction	COF 对侧向 COF 侧		
23	Power consumption	TBD	mW	
24	Life time	290h	LT95	
25	Panel Thickness	0.5	mm	
25	Polarizer Type	0.147	mm	
26	SCF	0.13	mm	
27	Brightness	800	cd/m	
28	contrast ratio	100000:1		
29	Color shift (L/R/U/D 30°)	4	*JNCD*	
30	Operation Temperature	-40~+70	deg	
31	Storage Temperature	-40~+80	deg	

2 Mechanical Drawing

2.1 Module Drawing

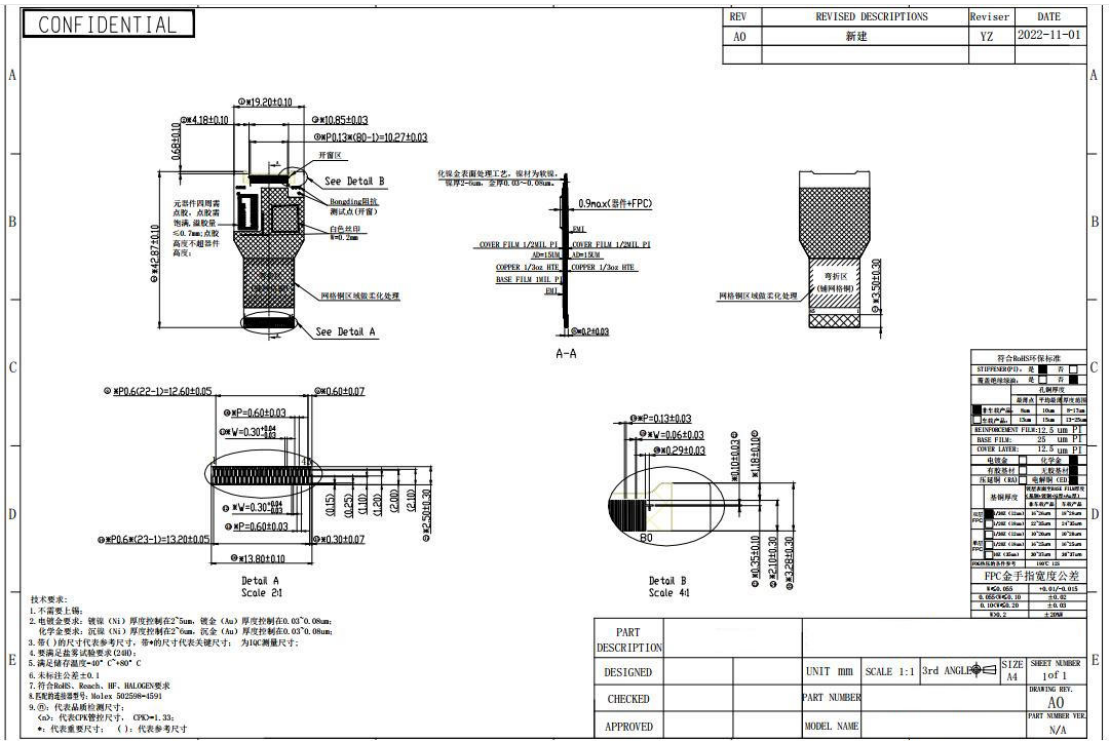
Drawing name	Version	ME Engineer	Change content	Update date
Display Module Drawing	A3			20221207



2.2 FPC schematic Drawing

Drawing name	Version	MD Engineer	Change content	Update date
M-FPC schematic Drawing	A0			2022-11-01

MFPC



3 Optical Specifications

Test condition：VCC= 3.3V, VDDIO=1.8V , Ta=25℃

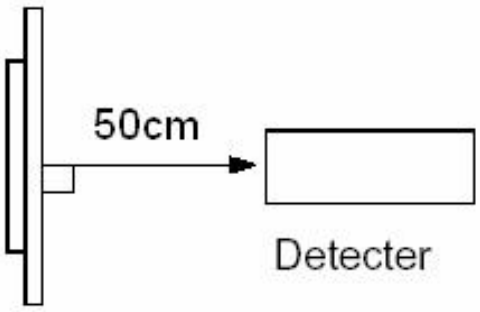
Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Luminance (with pol&lens)		Normal mode Bp	θ=0° ϕ=0°	720	800	880	cd/m2	
Uniformity		ΔBp		90	--	--	%	
Viewing Angle	Left	θL	Cr≥10	80	--	--	deg	
	Right	θR		80	--	--		
	Top	ψT		80	--	--		
	Bottom	ψB		80	--	--		
Contrast Ratio		Cr	θ=0° ϕ=0°	10000 0：1		--	-	
Response Time		Tr		--	--	2	ms	
		Tf		--	--	2	ms	
		Tgray		--	--	2	ms	
Color Coordinate of CIE1931	Red	x	θ=0° ϕ=0°	0.660	0.680	0.700	色标表根据具体项目定，会有不同	
		y		0.300	0.320	0.340		
	Green	x		0.205	0.245	0.285		
		y		0.675	0.715	0.755		
	Blue	x		0.121	0.141	0.161		
		y		0.023	0.043	0.063		
	White	x		0.280	0.300	0.320		
		y		0.290	0.310	0.330		
Color temperature		CT		7000	7500	8000	K	
Flicker		amount	60HZ @Interval screen(间隔画面)	--	--	-30	dB	
		amount	60HZ @255Gray	--	--	-50	dB	
		amount	45HZ, @255Gray	--	--	-40	dB	
		amount	30HZ, @255Gray	--	--	-30	dB	
		amount	15HZ, @255Gray	--	--	-30	dB	
Gamma								

	Normal mode		2.0	2.2	2.4		
Reflectance (With lens)	Rf	550nm	--	--	5.5	%	
Transmittance (Without lens)	Tr	400~700nm	--			%	
Polarization direction of front polarizer	PdF		--	135	--	deg	
Color shift		θL=30°	--	3	4	JNCD	
		θR=30°	--	3	4	JNCD	
		ψT=30°	--	3	4	JNCD	
		ψB=30°	--	3	4	JNCD	
OLED lifetime	LT95*(Without lens 800nit)	At 25℃,with white color pattern	290	--	--	hrs.	

3.1: Luminance measurement

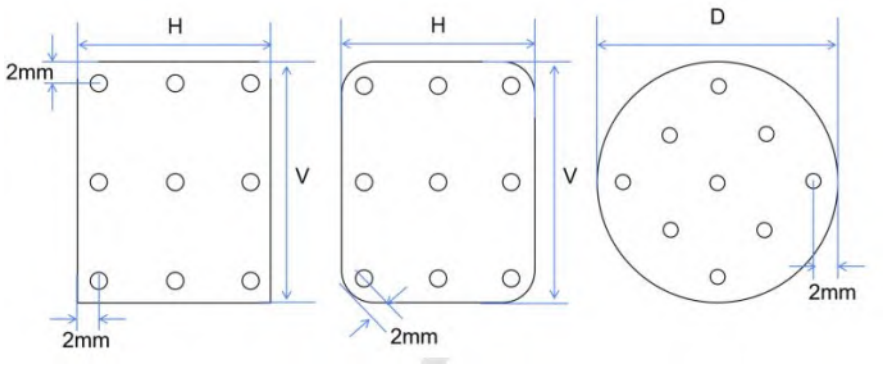
The test condition is at 25℃ and measured on the surface of OLED module.

- The data are measured after OLEDs are lighted on for more than 5 minutes and displays
- equipment CS2000/CS2000A or similar equipments (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measured value at the center point of panel must be after more than 5 minutes while light up



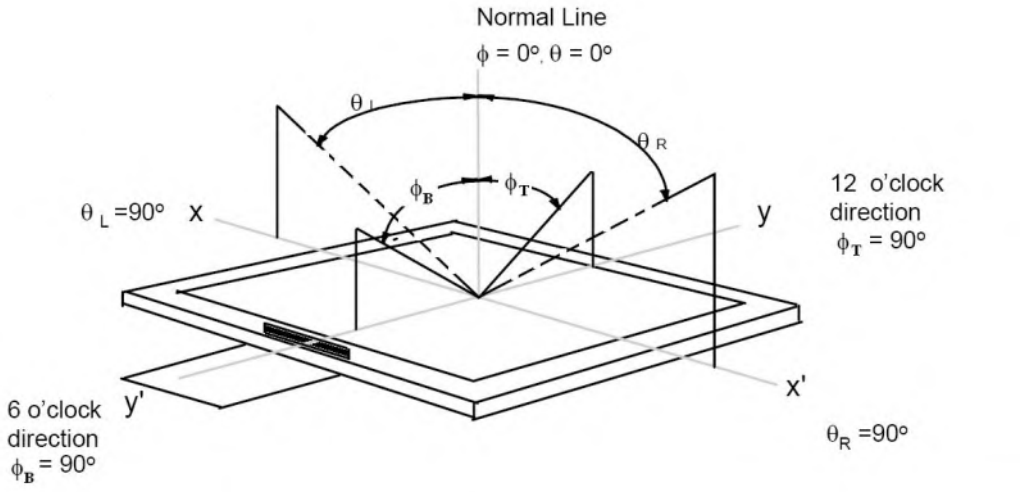
3.2: Uniformity

- The test condition is at 25℃ and measured on the surface of display module
- Measurement equipment: CS2000/CS2000A or similar equipment.
- The luminance uniformity is calculated by using following formula.
  △Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 9 measured spots
- Bp (Min.) = Minimum brightness in 9 measured spots.



3.3: The definition of Viewing Angle

Refer to the graph below marked by *θ* and *Φ*



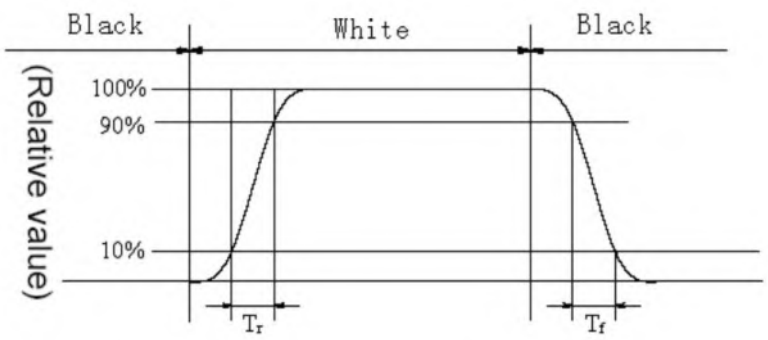
3.4: The definition of Contrast Ratio (Test OLED using CS2000/CS2000A or similar equipments):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance is at “White” state}}{\text{Luminance is at “Black” state}}$$

(Contrast Ratio is measured in optimum common electrode voltage. Black state display pure black color and luminance<0.002nits.)

3.5: Definition of Response time. (Test module using DMS 803 or similar equipment):

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(Voltage falling time) and from “white” to “black”(Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 80% of amplitudes. Refer to figure as below.



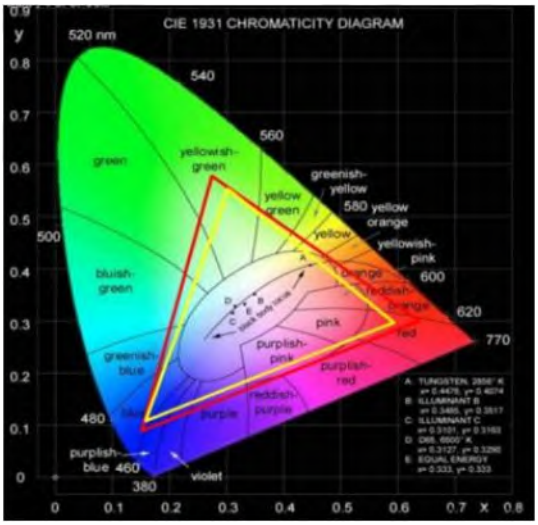
Response time of gray to gray:

- Measurement equipment: DMS803 or similar equipment.
- Test method: we define 8 grays L0-L7, the grays of L0-L7 were defined as:0,36,73, 109, 146, 182, 219, 255. The output signals of photo detector are measured when the input signals are changed from “Lx” to “Ly”, x, y= [0, 7]. The response time is defined as the time interval between the 10% and 90% of amplitudes. The result of the test can be noted as below:

	L0	L1	L2	L3	L4	L5	L6	L7
L0	■							
L1		■						
L2			■					
L3				■				
L4					■			
L5						■		
L6							■	
L7								■

3.6: Definition of Color of CIE Coordinate and NTSC Ratio.

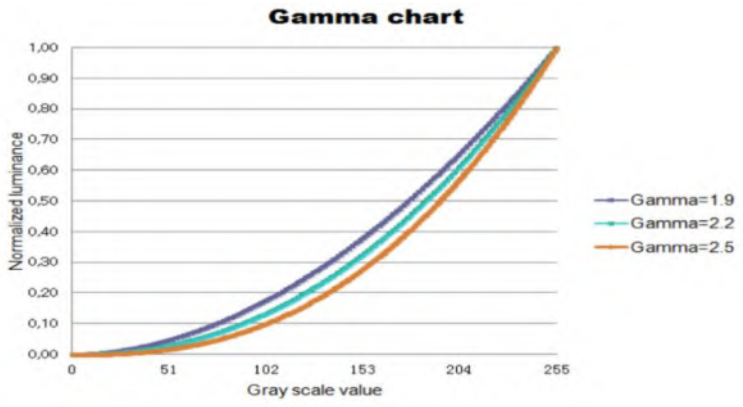
$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$



3.7: gamma curve control

- For gamma curve control, request as below:
- the whole curve's tolerance must control within +/-0.3, will test the gray scale below: 0~255gray, interval 8 gray (0,8,16,24……255)
- According to below formula chart the curves

$$TR\%x = \sqrt{\frac{Gx - G0}{G255 - G0}}$$

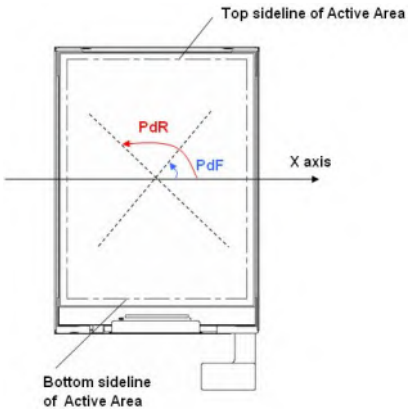


3.8: Reflectance Ratio

- Measurement equipment: Hunter Lab USPRO, Konica-Minolta CM-3600
- Measurement parameter：Reflectance Ratio @550nm

3.9 Polarization Direction Definition

- Viewing direction is normal user viewing direction which is vertical to the display surface
- The X axis is defined as parallel line to top&bottom sidelines of the Active Area
- PdF which is marked in blue arrow is polarization degree of Front polarizer
- The polarization degree parameter must be indicated in range of 0deg to 180deg according to above definition
- The angle definition of Polarization： The angle between polarized axis of Polarizer and zero of LCD
- Reference： Transmission axis 90deg for normal LCD POL; 45deg for normal OLED POL;TBD for sunglass POL;



Polarization Definition

3.10: Color Shift JNCD

- For JNCD measure:
- Fix on one pattern like white pattern,
- On the condition θ=0 F=0°, we can get the color coordinate (u1', v1') and onθL=30° we can get another color coordinate (u2', v2')
- Delta = Square Root((u2' - u1')^2 + (v2' - v1')^2)
- JNCD stands for "Just Noticeable Color Difference"
- For the (u', v') color space JNCD=0.0040.
- 2JNCD means Delta u'v'<0.0080
- For color shift we need to measure white/red/green/blue pattern.

3.11 OLED lifetime

- Test samples 5pcs;
- Measurement equipment: CS2000/CS2000A or similar equipment.
- At room temperature(25℃), light the module with typical value brightness, display a white pattern,
- To record the brightness every 24 hours.
- LT95>290h.

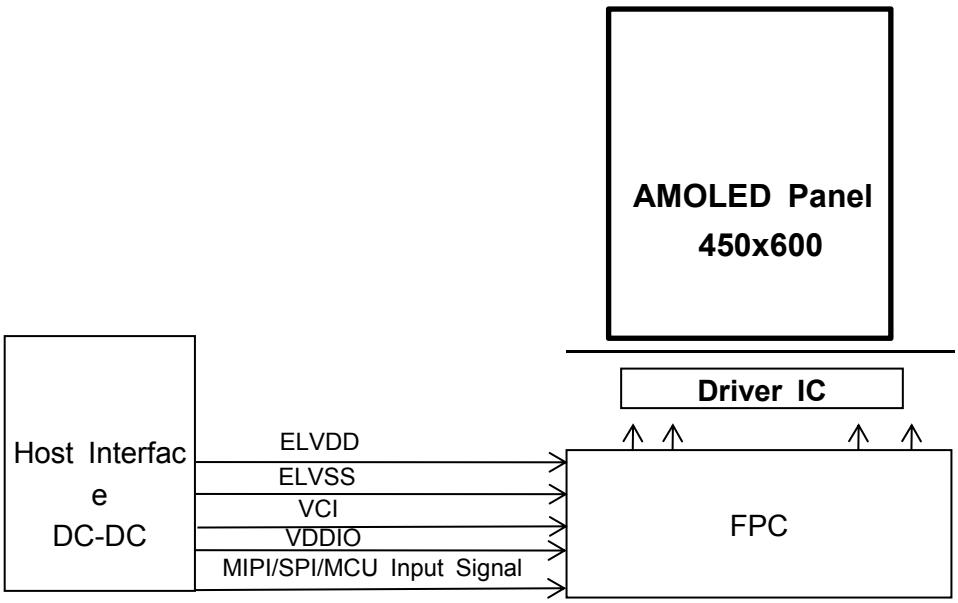
4 Pin Assignments

AMOLED Interface Definition

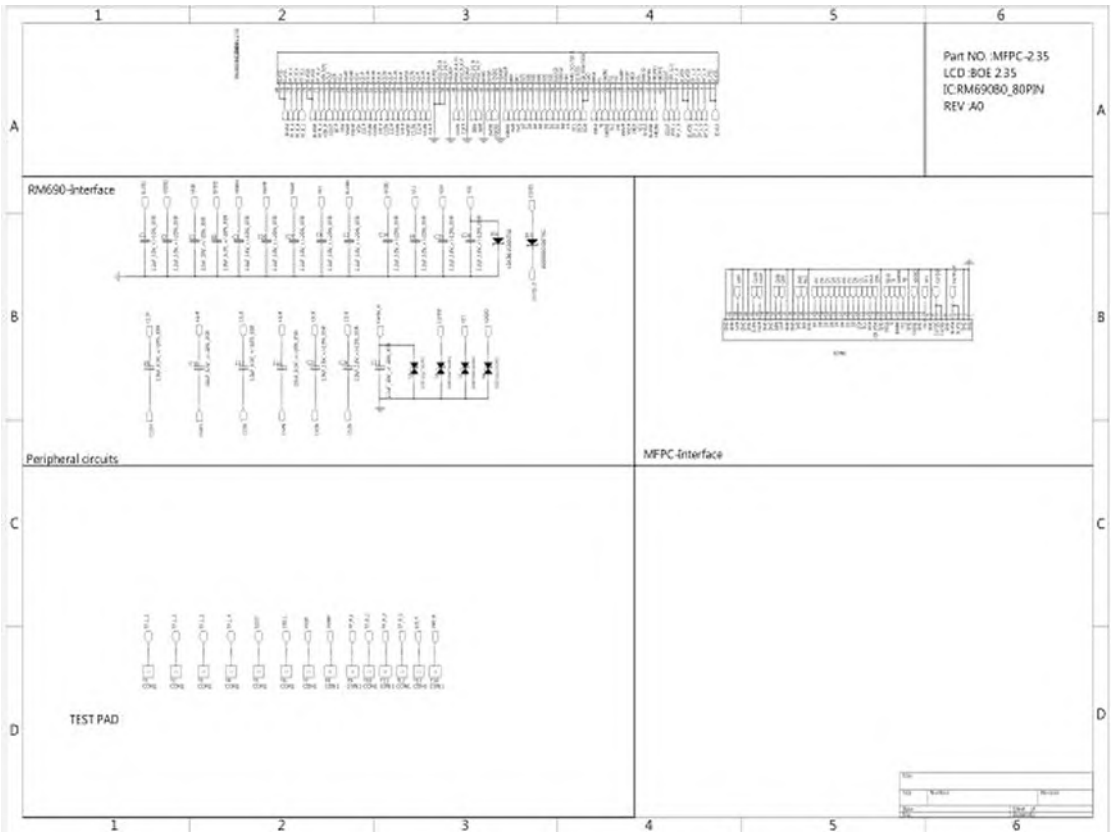
AMOLED Pin No.	Symbol	I/O	Function
1	GND	Power	Ground.
2	GND	Power	Ground.
3	ELVSS	Power	Negative Power supply for Panel
4	ELVSS	Power	Negative Power supply for Panel
5	GND	Power	Ground.
6	ELVDD	Power	Positive Power supply for Panel
7	ELVDD	Power	Positive Power supply for Panel
8	GND	Power	Ground.
9	VCI	Power	Power supply for display driver IC analog system.
10	GND	Power	Ground.
11	VDDIO	Power	Power supply for display driver IC interface and logic system
12	GND	Power	Ground.
13	TE1	O	IC Status active reporting pin.
14	SWIRE	O	Swire protocol setting pin of Power IC
15	TE	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.
16	RESX	I	Display driver reset, must be applied to properly initialize the chip. Signal is active low.
17	GND	Power	Ground.
18	SDI_RDX	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. RDX: Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface.
19	DCX	I	Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F.
20	SCL	I	WRX : Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F.
21	CSX	I	Chip select input pin (“Low” enable) in 80-series

			MPU I/F and SPI I/F.
22	D0	I/O	8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F.
23	D1	I/O	
24	D2	I/O	
25	D3	I/O	
26	D4	I/O	
27	D5	I/O	
28	D6	I/O	
29	D7	I/O	
30	GND	Power	Ground.
31	IM1	I	Interface type selection.
32	IM0	I	
33	GND	Power	Ground.
34	GND	Power	Ground.
35	D0P	I/O	Differential data signals if MIPI interface.
36	D0N	I/O	Differential data signals if MIPI interface.
37	GND	Power	Ground.
38	GND	Power	Ground.
39	CLKP	I	Differential clock signals if MIPI interface.
40	CLKN	I	Differential clock signals if MIPI interface.
41	GND	Power	Ground.
42	GND	Power	Ground.
43	MTP	Power	MTP programming power supply. Must be left open or connected to GND in normal condition
44	GND	Power	Ground.
45	GND	Power	Ground.

5 Schematic Circuit Diagram



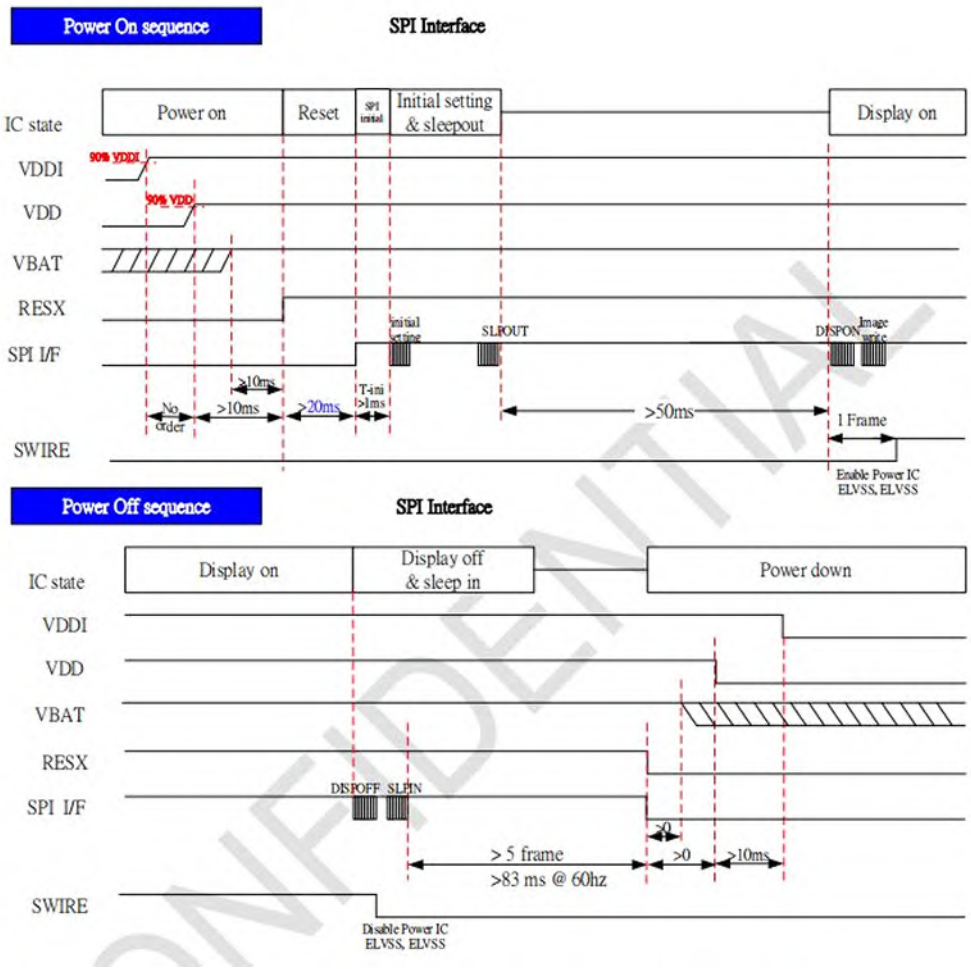
MFPC Schematic Diagram



6 Timing Characteristics

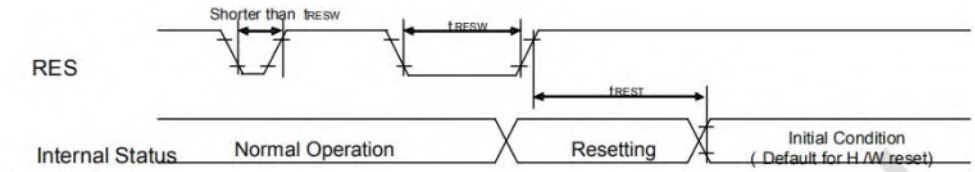
6.1 Power on/off Sequence

6.1.1 Display panel Power on sequence



6.2 Reset Timing Sequence Requirement

6.2.1 Display panel reset timing:

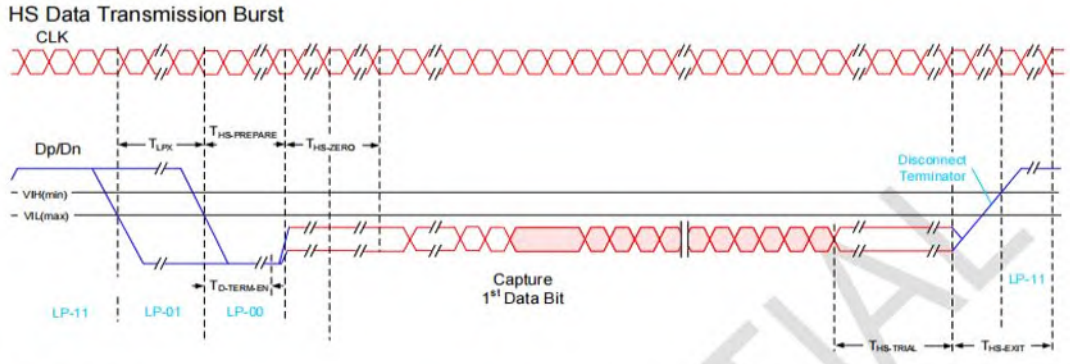


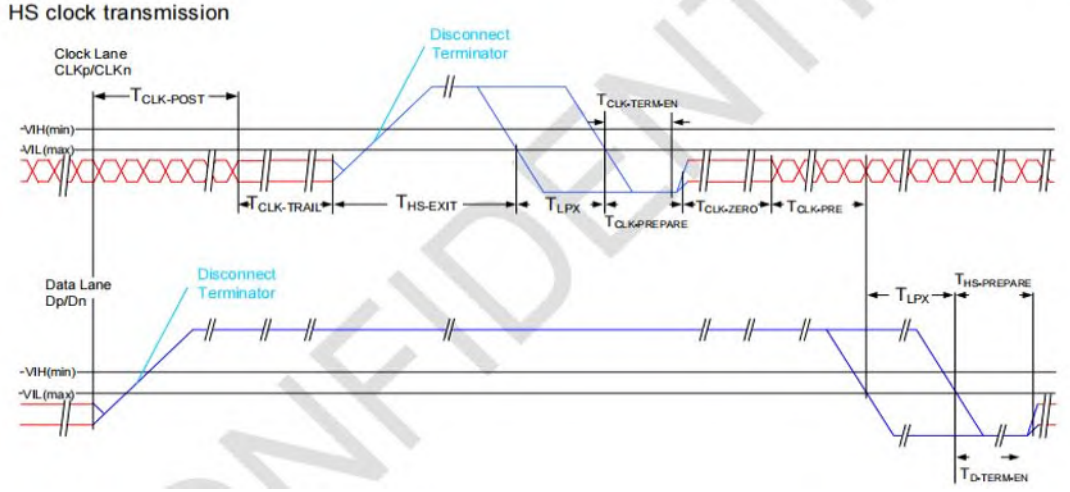
Reset input timing:
VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

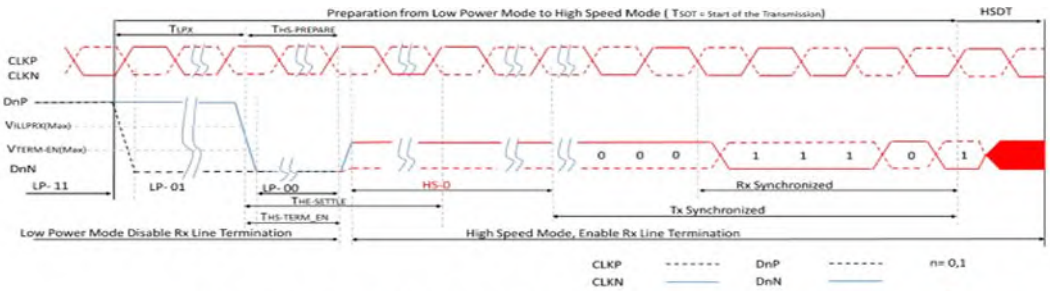
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	30	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	20	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

6.3 Communication Interface timing

6.3.1 MIPI-DSI 1 lane Interface Characteristics







Data Lanes from High Speed Mode to Low Power Mode Timing

Data Lanes from Low Power Mode to High Speed Mode Timing

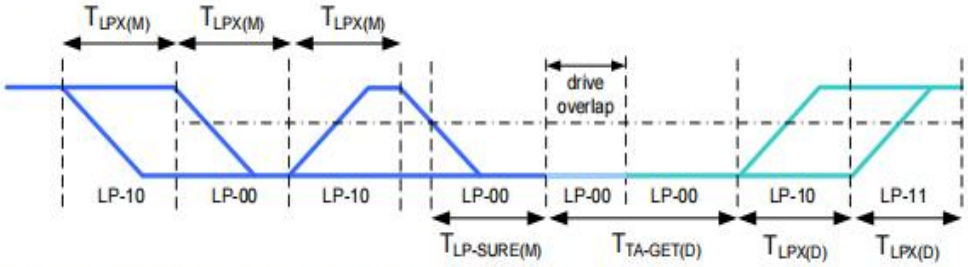
Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	$T_{HS-TREM-EN}$	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0, and 1*

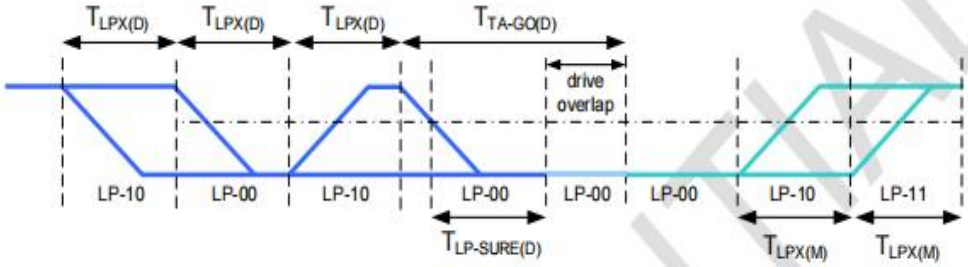
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



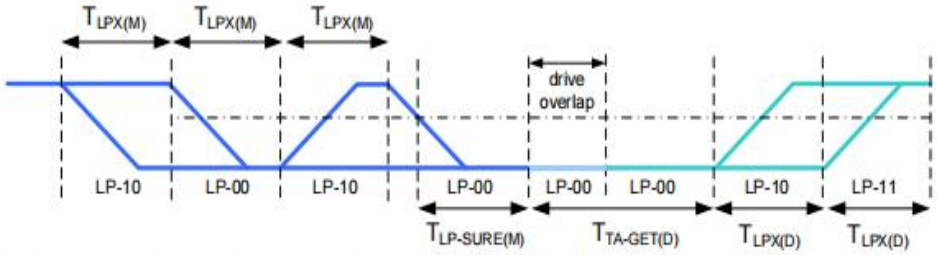
Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

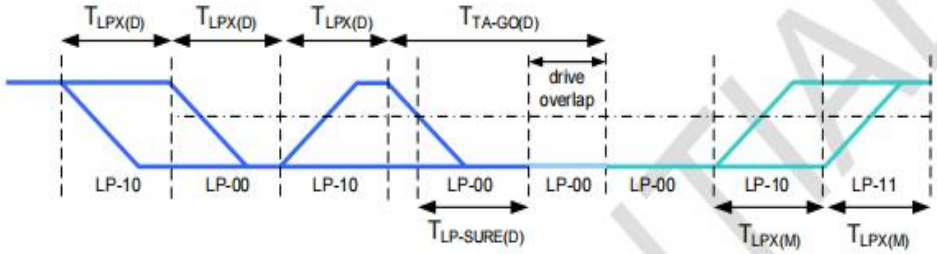
Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

6.3.2 Initial sequence Characteristics

MIPI SPEED :
500Mbps

mipi 0x15 0xFE 0x00;
mipi 0x39 0x2A 0x00 0x00 0x01 0xC5;
mipi 0x39 0x2B 0x00 0x00 0x01 0xC5;
mipi 0x15 0x35 0x00;
mipi 0x15 0x51 0xFF;
mipi 0x05 0x11;
wait 120ms;
mipi 0x05 0x29

7 Electrical Specifications

7.1 DC Characteristics Requirements

Item	Symbol	Values			Unit	Remark
		Min	Type	max		
Analog power supply Vo	VCI	2.7	3.3	3.6		
I/O Supply Voltage	VDDIO	1.65	1.8	3.3	V	
OLED input voltage	ELVDD	2.0	3.6	6	V	
OLED input voltage	ELVSS	-4.7	-3.6	-0.4	V	
VCI_EN Voltage	VCI enable signal	VIL:0.4V VIH:1.2V				
Input High Voltage	VIH	0.8*VDDI	--	VDDI	V	
Input Low Voltage	VIL	0	--	0.2*VDDI	V	
Output High Voltage	VOH	0.8*VDDI	--	VDDI	V	
Output Low Voltage	VOL	0	--	0.2*VDDI	V	
Frame Frequency (60Hz)	frame	58	60	62	HZ	

7.2 Power Consumption of Display

Power Supply: **VDDIO=1.8V VCI=3.3V**

Item		Symbol		Condition	Symbol	Min.	Typ.	Max.	Uni	Remark
ELVDD		ELVDD		Normal	-	-	3.6	-	V	External Power
ELVSS		ELVSS		Normal	-	-	-3.6	-	V	External Power
VCI		VCI		-	-	-	3.3	-	V	
VDDIO		VDDIO		-	-	-	1.8	-	V	
Power Consumption	Display on mode (Normal)	IC	VCI	100% Pixel On,800nits, 60Hz	Ivci		TBD		mA	
					Pvci		TBD		mW	
			VDDIO		Ivddio		TBD		mA	
					Pvddio		TBD		mW	
		Panel	EL		I_{ELVDD}		TBD		mA	
					I_{ELVSS}		72.2		mA	
					Pnl		TBD		mW	
Frame Rate		F_{frm}		-40℃~80℃	F_{frm}	55.2	60	64.8	Hz	
				25℃		58.2	60	61.8	Hz	

8 Reliability TEST

ITEM		Condition
Environment Reliability	Thermal Humidity Operating test (THO)	+70℃, 90%RH, 240h
	Low Temperature Operating test (LTO)	-40℃, 240h
	High Temperature Operating test (HTO)	80℃, 240h
	High Temperature Storage test(HTS)	80℃, 240h
	Low Temperature Storage test (LTS)	-40℃, 240h
	Thermal Cycle Storage test (TST)	-40℃~+80℃, storage, 1h/cycle, 100cycle